LET Dependence of Gate Oxide Breakdown of SiC-MOS Capacitors due to Single Heavy Ion Irradiation

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Abstract

The currents through the gate oxide of the 4H-Silicon Carbide (SiC) Metal Oxide Semiconductor (MOS) capacitors at the accumulate condition were measured during heavy ion irradiation. Linear Energy Transfer (LET) dependence of the critical electric field (E_{cr}) at which the dielectric breakdown occurs in 4H-SiC MOS capacitors was studied. It was revealed that E_{cr} decreases with increasing LET. E_{cr} for SiC became higher than that for Si. This suggests that SiC MOS devices are promising candidates for high SEGR resistant devices.

1. Introduction

Galactic cosmic rays such as high energy heavy ions incidence in Metal Insulator Semiconductor (MIS) devices cause the catastrophic failure in the gate dielectric by amount of induced carrier. This phenomenon is well known as Single Event Gate Rupture (SEGR). In previous studies of SEGR in Silicon (Si) Metal Oxide Semiconductor (MOS) devices [1-7], it was reported that the probability of SEGR increased with increasing the electric field applied to devices. In addition, even on the ground, the issue of SEGR due to neutrons created by cosmic rays arises in Si MOS power devices operated under very high electric field.

Silicon Carbide (SiC) is applicable to the high power devices with high radiation hardness. Ohshima et al. [8] clarified the Total Ionizing Dose (TID) effect of SiC MOS Field Effect Transistors (FETs), and they showed SiC MOSFETs have higher radiation resistance than Si MOSFETs. However, SEGR in SiC MOS devices has not yet been understood. Since SiC power devices are expected to be operated under higher electric field than Si power devices, it is very important to study about SEGR in SiC devices.

In this study, by measuring the leakage current through the gate oxide of 4H-SiC MOS capacitors during heavy ion irradiation, we investigate the Linear Energy Transfer (LET) dependence of the critical electric field (E_{cr}) at which SEGR occurs in SiC MOS capacitors.

2. Experimental

The MOS capacitors samples (gate electrode either 180 or 280 μm in diameter) used in this study were fabricated on n-type epitaxial layer (4.9 μm thick). Epitaxial layer was grown on an n-type 4H-SiC substrate (8° off, Si-face). The donor concentration of the epitaxial layer was 3.7×10^{15} cm^{-3}. The MOS capacitors were fabricated by the following processes. Firstly, the field oxide at a thickness of 180 nm was formed on the sample surface by a pyrogenic oxidation process (H_2:O_2 = 1:1) at 1100 °C for 180 minutes. Next, the field oxide with a diameter of either 180 or 280 μm was removed by a conventional photolithography technique and a wet etching technique using buffered hydrofluoric acid (HF:NH_4F = 1:5). Next, the gate oxide was grown on the sample by pyrogenic oxidation at 1100 °C for 60 minutes. After the oxidation, the samples were cooled from 1100 to 900 °C for 1 hour under an argon (Ar) atmosphere. Then, re-oxidation under the pyrogenic condition was carried out at 900 °C for 15 minutes. The thickness of the gate oxide was estimated to be from 65 to 80 nm from Capacitance - Voltage (C-V) measurements. Aluminum (Al) electrodes with a thickness of 200 nm were formed on the gate oxide using Al evaporation followed by a conventional lift-off technique. Finally, Al bonding pads and interconnections (between the bonding pad and the gate electrode) were formed using Al evaporation followed by a conventional lift-off technique [9]. The leakage currents through the gate oxide of the samples were below 1.0 pA at an accumulate condition of 3 MV/cm. The flat band voltage shifts (ΔV_{FB}) of samples were estimated to be from 2.86 to 5.17 V from C-V characteristics.

The samples were irradiated with Nickel (Ni) at 9 and 18 MeV, Krypton (Kr) at 322 MeV, and Xenon (Xe) at 454 MeV. The LETs, ion species, energies, range in SiC and flux used in this study are described in Table 1. We used a 3MV tandem accelerator for Ni ion irradiation and an AVF cyclotron accelerator for Kr and Xe ion irradiation. Fluxes of ions were controlled to be low enough to avoid degradation of device characteristics due to the TID effect.

The leakage current of sample irradiated with ion at low electric field (E < 2MV/cm) did not change compared with pre-irradiation. This suggests that the TID effect did not affect to measurement. The leakage current through the gate oxide of the MOS capacitors was monitored under direct current (DC) biases. The gate oxide was applied DC biases from 20 to 100 V toward the accumulation condition. DC bias step rate was 0.2 V per 6 seconds. The compliance current set as 1 mA which the destruction of gate oxide occurs.

Table 1. List of ions and their characteristics.

LET [MeV • cm^2/mg]	Ion species	Energy [MeV]	Range [μm]	Flux [/cm^2 • sec]
0	No Ion	--	--	--
14.6	Ni	9	3.63	3.46×10^4
23.8	Ni	18	5.04	3.87×10^4
42.2	Kr	322	27.2	4.43×10^3
73.2	Xe	454	35.7	2.98×10^3

3. Results and Discussion

Figure 1 shows the leakage currents through the gate oxide of the 4H-SiC MOS capacitors as a function of the electric field applied to the gate oxides with and without ion irradiation. The effect of ΔV_{FB}, which was evaluated from C-V measurements, was considered in the estimation of the electric field shown in Fig. 1. The leakage currents for all samples sharply increase to compliance current (1 mA) after gradually increase of leakage current. In this study, the value of the electric field at leakage current of 1 mA is defined as E_{cr}. The E_{cr} of samples irradiated with ions are smaller than that of non-irradiated one (E_{cr0}), and decrease with increasing LETs.

Figures 2 (a) and (b) show optical microscope images of the gate electrodes of SiC MOS capacitors irradiated with Ni ions at 18 MeV and Xe ions at 454 MeV, respectively. As shown in Figs. 2 (a) and (b), the partial destruction of the Al electrodes are observed. Since the sharp increase in the leakage current through the gate oxide was observed (as shown in Fig. 1), the partial broken of the Al electrodes of SiC MOS capacitors is thought to be created by following steps. When an n-type MOS capacitor is irradiated with high LET heavy ions, the large amounts of electron-hole pairs are generated in SiC. Since the n-type SiC MOS capacitor is biased toward the accumulate condition, electrons generated near the interface between gate oxide and SiC drift to the interface. On the other hand, holes generated near the interface move away from the interface due to drift. Then the electric field applied to gate oxide increases by electrons collected at the interface. If the electric field in gate oxide exceeds the critical electric field, the breakdown of gate oxide occurs. As a result, a large current flow at the breakdown point(s), and the Al electrode is broken due to a large current. Thus, the spots observed in Figs. 2 (a) and (b) mean the generation points of SEGR. It is also mentioned that when the partial broken of the Al electrode occurred at the edge of the electrode connected to a bonding pad, a sudden drop in the leakage current was observed (not shown here). In such a case, although the sharp increase in the leakage current is not observed, we also defined the electric field at the sudden drop in the leakage current as E_{cr}.

Figure 3 shows the LET dependence of E_{cr} irradiated with ions. The values of E_{cr} reported for Si MOS capacitors are also plotted in the figure for comparison [2, 3]. The E_{cr0} for SiC was lower than that of Si reported by Sexton *et al.* However, as shown in Fig. 3, they also reported that the value of E_{cr0} depended on the thickness of SiO_2 and the thinner oxide showed the higher E_{cr0} [2]. Pre-irradiation breakdown in the gate oxide depends on the quality of the oxide, and the oxide thickness is fundamentally a function of the quality of the gate oxide. As mentioned above, the thickness of the gate oxide in this study ranged from 65 to 80 nm. Therefore, the smaller value of E_{cr0} for SiC is due to thicker oxide. As shown in Fig. 3, the values of E_{cr} for both SiC and Si decrease with increasing LET. Since ions with higher LET can generate larger amounts of electron-hole pairs in a sample, larger increase of the potential applied to the gate oxide can be induced by the incidence of ions with higher LET. This fact suggests that SEGR easily occurs at lower electric field by ions with higher LET. It is found that the gradient of the E_{cr} – LET curve for SiC is smaller than those for Si. This result can be explained in terms that electron – hole pair creation energy ($E_{e\text{-}h}$) is different between SiC and Si. The value of $E_{e\text{-}h}$ for SiC (7.8 eV) is larger than that for Si (3.6 eV). The result obtained in this study might relate to the difference of E_{cr}. In other words, the number of electron-hole pair generated in SiC is smaller than that in Si when the same ion (the same LET) penetrates. As shown in Fig.3, our study was also compared with Si vertical power MOSFETs (at the drain source voltage is zero) which were reported by Wheatley *et al.* [3]. Wheatley's E_{cr} was consistently lower than our results. This results suggested that the MOSFETs were needed several post-gate process for device fabrication which may give more defects in the gate oxide. Thus, this comparison is not necessarily justified. These results suggest that SiC MOS devices have a potential as the application for SEGR resistant devices.

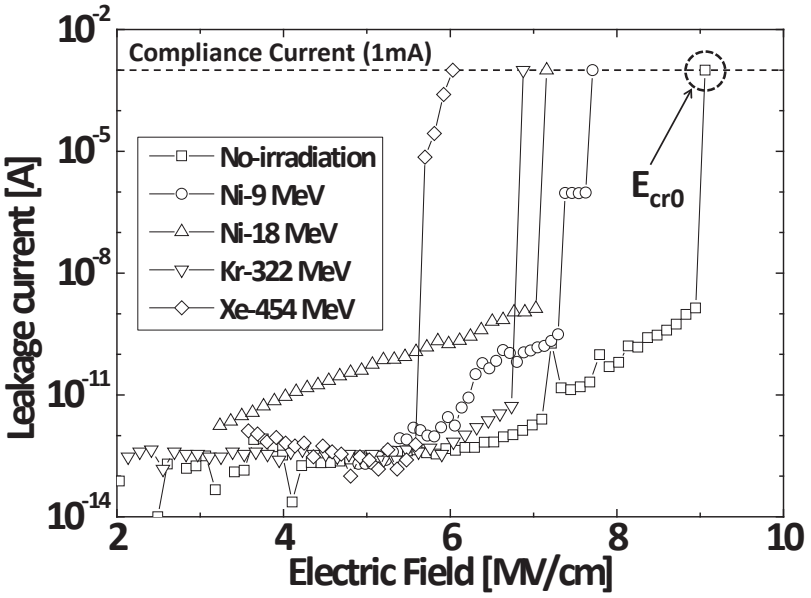

Fig. 1: Leakage currents of SiC MOS capacitors with and without heavy ion irradiation.

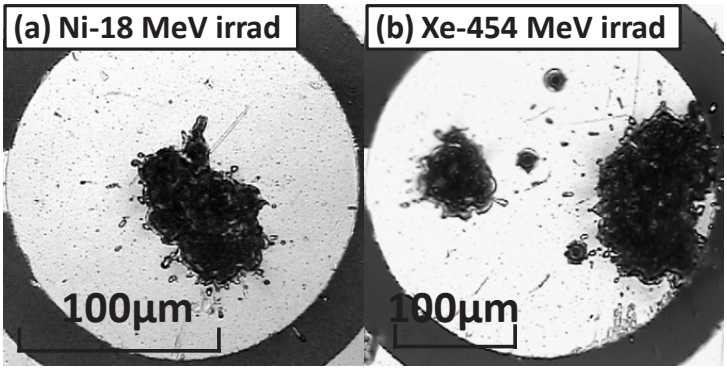

Fig. 2: Optical microscope images of electrode in MOS capacitor irradiated with Ni-18 MeV and Xe-454 MeV.

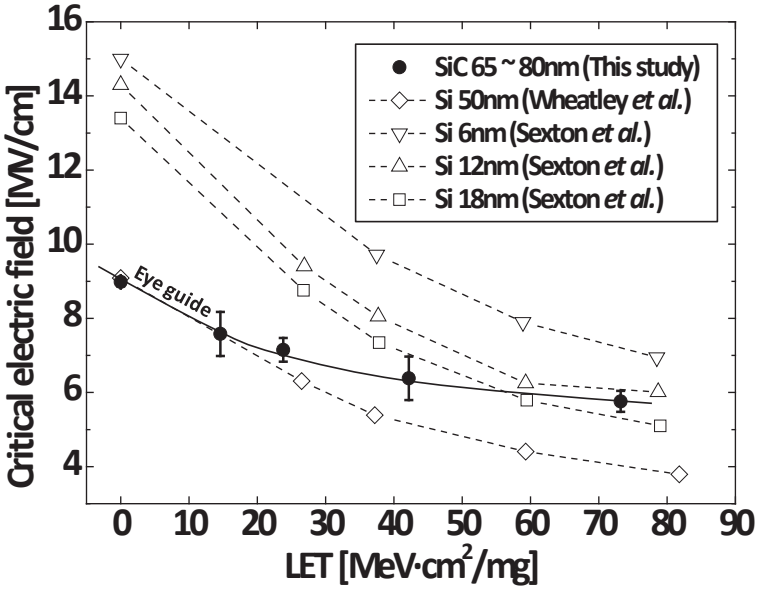

Fig. 3: LET dependence of SEGR electric field in SiC and Si MOS capacitors.

Summary

MOS capacitors were fabricated on an n-type epitaxial layer grown on an n-type 4H-SiC substrate. The currents observed through the gate oxide of the MOS capacitors biased toward the accumulate condition were measured during heavy ion irradiation. LET dependence of E_{cr} in 4H-SiC MOS capacitors under ion irradiation was studied. The E_{cr} for SiC MOS capacitors decreases with increasing LET. The gradient of the E_{cr} – LET curve for SiC is smaller than those for Si. This suggests that SiC MOS devices have a potential as the application for SEGR resistant devices.

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