Single Event Effects E - 4

# Applicability of redundant pairs of SOI transistors for analog circuits

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## Abstract

Redundant pairs of SOI transistors have been utilized as a Radiation Hardening-By-Design technique and their applicability was subsequently extended for analog circuits. In this paper, the principle of the SET free inverter (SFI) operation is extended to analog circuits such as current mirror circuits and has been successfully demonstrated with a phase-locked loop circuit intended for use in ASICs, which includes some analog circuit blocks, such as the current mirror, differential amplifiers and so on.

## 1. Introduction

Single-event transient (SET) pulse in nanometer-scale integrated circuits, which is caused by high energy heavy ions and protons in space radiation, is a serious problem for electronic equipment intended to be operated in space. Much time has been spent extensively studying many mitigation techniques such as triple modular redundancy (TMR) [1].

The SET free inverter (SFI) circuit is one such mitigation technique and only applicable to SOI process technology [2]. However it has a unique ability to prevent SET pulse generation essentially via the circuit itself. Conversely, however, no other techniques can prevent the generation of SET pulses, meaning the pulses must be rejected or suppressed by additional voting or filtering circuits to eliminate their effects in this case and the additional timing penalty may impair the system operating frequency. A trade-off is thus needed between operating frequency and SEU immunity. The principle of the SFI circuit is easily extended to all other combinational and sequential logic circuits and successfully applied to application specific integrated circuits (ASICs) [3] including a micro-processor unit (MPU) for space applications.

In this paper, the principle of SFI operation is also extended to analog circuits such as current mirror circuits and has been demonstrated with a phase-locked loop circuit intended for use in ASICs, which includes some analog circuit blocks, such as the current mirror, differential amplifiers and so on.

## 2. Principle of the SET free inverter

The SFI circuit is obtained by replacing each transistor in a standard CMOS inverter with a pair of redundant transistors, i.e. each of the P- and N-channel transistors is replaced by a pair of P- and N-channel transistors connected in series as shown in Fig. 1(a). The supply current flow in its static condition is blocked by the redundant pair transistors and the potential of each node is divided by the transistors as shown in Fig. 1(b) in principle. Upon the incidence of high energy particles on one of the pair transistors, the voltage applied between the drain and source of the transistor is reduced, whereupon the voltage is transferred to another transistor in the pair and a very small amount of charge is displaced. It should be noted that the voltage transfer mechanism between the redundant pair of transistors only works as expected with SOI process technology because the transistors must be isolated by insulator instead of a reverse-biased p-n junction, as in bulk technology.

The worst case transient response is estimated by a circuit simulator such as SPICE, with a switch to short the drain and source [4]. For standard CMOS circuits, the series resistance and close time duration of the switch should be adjusted to simulate the response for the intended LET value of the incident ions. However, the switch can simply be closed with a low contact resistance to estimate the worst case response for SFI circuits. Even if the switch is closed, there is no DC power supply path. For the SFI circuit shown in Fig. 1(a), implemented by a 0.15 μm fully depleted SOI (FDSOI) from the LAPIS semiconductor (former OKI), the worst voltage disturbance at the output terminal is observed with an ion strike on $M_{P2}$. The peak level and full width at the half maximum (FWHM) of the output voltage disturbance are plotted as a function of switch resistance in Fig. 2. The supply voltage was a nominal specified voltage of 1.5 V. The peak level of the disturbance is less than 150 mV and declines in the higher switch resistance region. In contrast, FWHM is increased at the region, but remains less than 20 ps, even if the resistance is increased up to 10 kΩ. The collected charge (total charge passed through the switch) remained almost constant over the resistance range (0.56 fC ± 0.2 %) and much less than the

deposited charge from an incident ion; for example, an average of 27 fC for an ion with a LET of 68.9 MeV/(mg/cm$^2$), assuming top silicon thickness of 40 nm. Obviously the disturbance level is too small and cannot be propagated to the subsequent stage of the logic circuit. The very small collected charge is attributable to the loss of voltage applied to the transistor just after being struck. This loss means the deposited charge in the body region is diffused for both the drain and source regions of the transistor, and the net current flow is very small, which is a key feature of the redundant pair transistors in SOI process technology.

For the hardening technique with the redundant pair transistors, simple attention is required for their layout. To obtain the required SET immunity, spacing of the gates is the key parameter. For the SOI technology utilized in this study, a minimum of 0.35 μm is required to achieve SET immunity up to LET of 68.9 MeV/(mg/cm$^2$) and the immunity was demonstrated experimentally [2]. The area of the pair is less than twice that of the single transistor.

The simulation results with SPICE were compared to those obtained by the 3D device simulator, HyDeLEOS [5], which generally provided more rigorous results. As a result, with a LET of 68.9 MeV/(mg/cm$^2$), it was confirmed that the simulation with SPICE as described above was applicable to estimate the worst case response of circuits utilizing redundant pair transistors.

## 3. Application to analog circuits

Redundant pair transistors are also applicable to analog circuit blocks, such as current mirror circuits. The latter are generally utilized to generate a constant current to drive other circuit blocks and comprise a matched pair of transistors as shown in Fig. 3(a). Each of the transistors in the pair can be replaced by a redundant pair of transistors as shown in Fig. 3(b). In analog circuits such as current mirror circuits, the transistors in the circuits are operated in linear mode and there are steady current paths in its static condition. However the key feature of the redundant pair transistors, i.e. substantially reducing the collected charge at the struck transistor, remains workable.

If one of the transistors in the redundant pair is shorted out by the switch as the SFI circuit to simulate SET pulse generation, the steady state current level also changes. The total collected charge can be measured similarly as for SFI circuits (the integrated current passed through the switch just after switch closure to steady state). For the circuits shown in Fig. 3, implemented by the same fabrication process discussed in the previous section, the worst case disturbance was observed where $M_{PL2}$ was struck. In this example, the output current was set to 100 nA with a nominal supply voltage of 1.5 V. The collected charge measured at the switch was also almost independent of the series resistance of the switch up to 10 kΩ and the values were around 2.5 fC. The collected charge gradually declined with increasing resistance beyond 1 kΩ and reduced to 2.0 fC at 100 kΩ. Therefore we can assume a worst case collected charge of around 2.5 fC. The peak current level passed through the switch and its FWHM (charge collection time) are plotted in Fig. 4. They were also almost independent of the series resistance of the switch up to 10 and 100 Ω and the values were around 360 ps and 6 μA, respectively. However, they increased or declined abruptly with switch resistance beyond 10 and 100 Ω.

Based on the above analysis, we can determine the switching condition to predict the worst case SET response, i.e. switch resistance of 10 kΩ and closure duration of 1 ns (around twice the FWHM). Fig. 5 shows the SET response for the current mirror circuits. For comparison, the SET response for a non-RHBD circuit is also indicated, which involved setting the switch resistance to 12.7 kΩ to adjust the collected charge to around 27 fC, i.e. a deposited charge for ions with LET of 68.9 MeV/(mg/cm$^2$) and a fixed switch closure duration of 1 ns. It is apparent that the SET response is greatly improved with the new RHBD technique, although the disturbance was not completely eliminated. It should also be noted that the result for the non-RHBD circuit is for ions with LET of 68.9 MeV/(mg/cm$^2$) and excludes any additional charge collection mechanism, such as bipolar amplification, meaning the result is not the worst case. In contrast, the result for circuits with a new RHBD technique is for the worst case with larger LET ions.

## 4. Verification with PLL circuits

### *4.1 PLL Circuit Design*

Phase-Locked Loop (PLL) circuits comprise several functional circuit blocks as shown in Fig. 6. The programmable divider (DM/DN/DO) and phase detector (PFD) are digital circuits, which can be hardened using SFI and derivative basic logic circuits. The remaining analog circuit blocks are voltage-switching charge pump (VCP), voltage-controlled current source (VCCS), and VCO. In this study, all these circuits were hardened utilizing the redundant pair transistors.

In a previous study, it was proposed to utilize VCP to improve immunity to the SET pulse [6]. In our design, a further simplified VCP circuit was applied. The VCP circuit is essentially similar to SFI and although the gates of the P- and N-channel transistors are independently controlled, they are never opened simultaneously. Therefore its SET immunity is expected to be as SFI.

VCO comprised a 5-stage ring oscillator in our design. The oscillator itself is a digital circuit and easily

hardened by utilizing SFIs. However, its output signal is not at a normal logic level and should be restored by a level converter (LC) for the subsequent circuit block, i.e. DO. The LC comprised a differential amplifier with redundant pair transistors, followed by 3 stages of SFIs to boost the output current. To restore the signal level, the differential amplifier is operated in the saturation region, i.e. its expected output voltage is 0 or $V_{DD}$ with a fast transition time. Accordingly, all transistors in the amplifier are operated as in the digital circuit and its SET immunity is expected to be as SFI.

VCCS is the most complicated analog circuit block in our PLL design and all the transistors are operated in linear mode. The circuit was also hardened using the redundant pair transistors. The circuit block comprised two current mirror circuits to boost the current supply capability to the VCO and gain control circuit. Its SET immunity was confirmed as described in the previous section.

The electrical performance of the PLL was evaluated with actual silicon. The power consumption was 2.4 mW at room temperature with power supply of 1.5 V. The cycle-to-cycle jitter was 70 ps rms at a VCO output frequency of 600 MHz.

*4.2 Heavy Ion Testing*

Heavy ions with LET of 3.4 to 68.9 MeV/(mg/cm$^2$) were used for the evaluation, the characteristics of which are listed in table II. These ions were irradiated normal to the chip surface and the supply voltage was set to a minimum of 1.35 V to obtain the worst case transient response. The input frequency was 10 MHz, VCO oscillated at an expected maximum operating frequency of 600 MHz, and the output frequency of PLL was set to 100 MHz for the experiments.

The cycle-to-cycle jitter was continuously monitored during irradiation by using 10Gs/s digital oscilloscope (TDS7104, Tektronix) with glitch detection trigger mode. The expected worst case cycle-to-cycle jitter (without irradiation) is an inherent characteristic of each PLL circuit and a function of operating time. For the irradiation test, the jitter attributable to the inherent characteristic should be excluded. In the actual test run, the prolonged or shortened cycles were defined as cycles with a deviation greater than |500ps| from the nominal cycle time. The jitter value is 7.1 and corresponds to the worst case jitter expected to be observed every 6 hours of PLL operation without irradiation.

The test data is shown in Fig. 7. For version A, erroneous output pulses (prolonged or shortened) for several contiguous cycles were observed. The saturated cross-section exceeded 10,000 μm$^2$. The output pulses are attributable to the non-RHBD VCCS. For version B, only single prolonged pulses were observed. The source of the error might be the non-RHBD LC. The observed saturated cross-section was around 20 μm$^2$ and in agreement with the area of LC as expected. Finally no erroneous pulse was observed up to LET of 68.9 MeV/(mg/cm$^2$) for version C.

## 5. Conclusions

In this paper, a new RHBD technique for analog circuits was proposed, which utilizes redundant pair transistors with SOI technology. The technique is very simple and incurs relatively little penalty in terms of power and area compared to TMR. Utilizing this technique, a PLL circuit with a maximum VCO frequency of 600 MHz was designed and fabricated with 0.15 μm Fully Depleted SOI technology. No erroneous pulse was observed up to a LET of 68.9 MeV/(mg/cm$^2$). The new RHBD technique was successfully demonstrated.

## Acknowledgments

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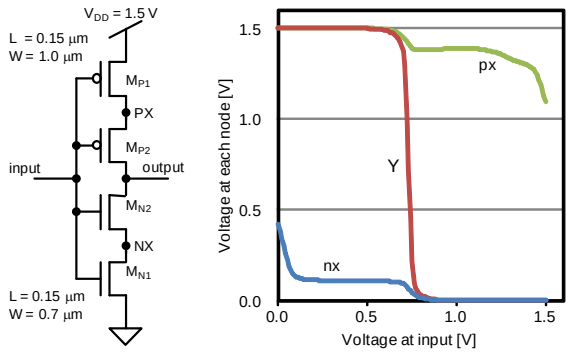



(a) (b)

Fig. 1. Schematic of SFI (a), and the Input-Output behavior of SFI (b).

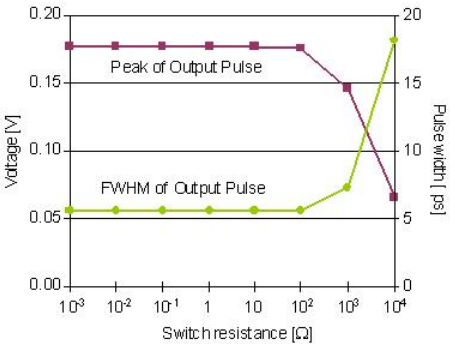
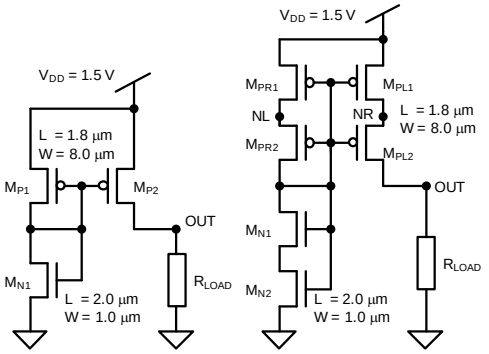



Fig. 2. Output voltage disturbance and as a function of switch resistance.




(a) (b)

Fig. 3. Current mirror circuit without RHBD (a), and Current mirror circuit with RHBD (b). Output current set to 100 nA for both circuits at $V_{DD}$ = 1.5 V.

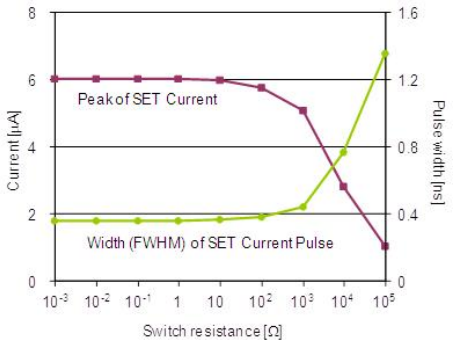



Fig. 4. Peak of the SET current pulse passed through the switch for the SET simulation and FWHM of the pulse as a function of the switch resistance.

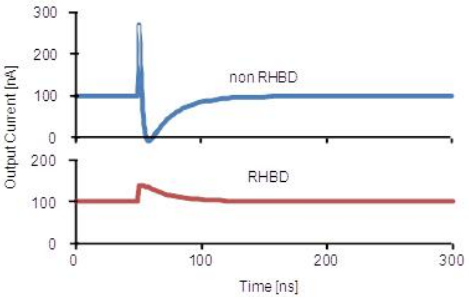
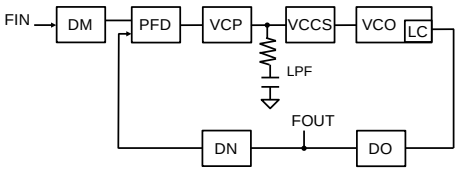



Fig. 5. SET response in the output current for RHBD and non-RHBD current mirror circuits.




DM/DN/DO: Programmable Divider circuits
PFD : Phase-Frequency Detector
V-CP : Voltage-Switching Charge Pump
LPF: Low-Pass Filter
VCCS : Voltage Controlled Current Source
VCO: Voltage Controlled Oscillator
LC: Level Converter

Fig. 6. Block diagram of PLL to demonstrate the new RHBD technique.

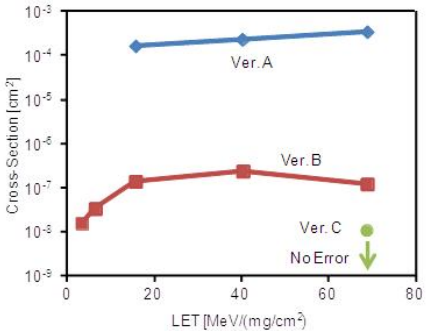



Fig. 7. Cross-section of erroneous output as a function of LET.

TABLE I
PLL DESIGN FOR SET IMMUNITY EVALUATION

| Block | Version A | Version B | Version C |
|---|---|---|---|
| V-CP | RHBD | RHBD | RHBD |
| VCO | RHBD | RHBD | RHBD |
| LC | no | no | RHBD |
| VCCS | no | RHBD | RHBD |
| Digital Blocks | RHBD | RHBD | RHBD |

TABLE II
CHARACTERISTICS OF IONS USED IN THIS STUDY

| Ion Species | Energy [MeV] | LET [MeV/(mg/cm²)] | Range [µm] |
|---|---|---|---|
| N | 53 | 3.6 | 49.1 |
| Ne | 70 | 6.5 | 38.9 |
| Ar | 137 | 15.8 | 36.1 |
| Kr | 289 | 40.3 | 37.3 |
| Xe | 398 | 68.9 | 35 |