Investigation of the SEE sensitivity of 90nm DICE based Flip-Flops using pulsed-laser testing methodology

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Abstract

This paper describes the evaluation result of the SEE sensitivity of 90nm DICE based flip-flops. Considering our past experimental results, modified DICE circuits were designed in order to minimize the charge sharing effect. The pulsed-laser SEE testing methodology was effectively utilized to identify the location of SEE sensitive areas. The comparison with the heavy ion irradiation test result were also discussed.

1. Introduction

Modern spacecrafts typically require a great variety of high-performance semiconductor devices to realize various types of space missions such as earth observations, telecommunications, planetary explorations, and so on. Recently, due to the requirements for higher density integration and device scaling, the logical circuits have been designed with <100nm design rule. Single-Event Upset (SEU) and Single-Event Transient (SET) phenomena are serious problems for those integrated circuits, because their supply voltage and the threshold to these events are also decreasing. In our past study[1,2], the effectiveness of Radiation Hardning by Design (RHBD) methodology for 90 nm CMOS process has been evaluated. Several types of Dual Interlocked Storage Cell (DICE) based Flip-flops have been designed and evaluated. As a result, by using the heavy ions AVF cyclotron, SEUs with relatively large cross-sections induced by the charge sharing[3-5] have been identified although normal angle irradiation test results showed excellent SEE tolerance.

In this study, modified DICE circuits were designed for 90nm CMOS process. The SEE sensitivity of these were also investigated. The pulsed-laser testing methodology was successfully utilized for the identification of potential vulnerabilities of test circuits.

2. Experimental

2.1 Descriptions of test circuits

The schematic diagram of DICE based flip-flop circuit evaluated in this study is shown in Fig.1. Considering our past experimental results[1-2], additional p-type transistors were inserted for each DICE elements to minimize the probability of multi-node SEUs caused by the penetration of ion particles with grazing angle. Filtering delay circuit was also applied in order to eliminate SET propagation on CLK signal line. Two types of circuit layout (Type A and Type B) were designed and tested as shown in Fig.2 (Because of the limitation of technology information disclosure, only the outline of layout was indicated in this figure). By using these element circuits, the memory block with a total size of 2k bit was constructed and installed to the test chip. Test chips were fublicated using Fujitsu's 90 nm bulk CMOS process.

2.2 Pulsed-laser test equipment

Usually SEE cross-sections are simply calculated from heavy ion irradiation test results by dividing a number of error bits by the total fluence. However this conventional method does not give us sufficient information to identify the location of SEE sensitive nodes. To overcome this issue, the pulsed-laser SEE test system, PULSYS-RAD made by PULSCAN (Bordeaux, FRANCE) was introduced and was used for this experiment (Fig.3). This was especially designed for the characterization of single-event effects in integrated circuits using picosecond laser pulses. The main characteristics of the light obtained from this equipment is shown in Table 1. In our experiment, DUT was mounted on the X-Y moving stage and scanned with 0.2 μm step width in order to identify the location of SEE sensitive area.

2.3 Sample preparation and test conditions

In general, modern semiconductor manufacturing processes use many metal layers to realize very large scaled integration circuits. In case of the laser testing, performing the irradiation from backside of the chip is indispensable to avoid the interfare of the laser penetration caused by metal layers. In our experiment, substrate of the test chip was thinned down to approximately 50 μm. After the thinning process, the chip was mounted to the small PWB board as shown in Fig.4.

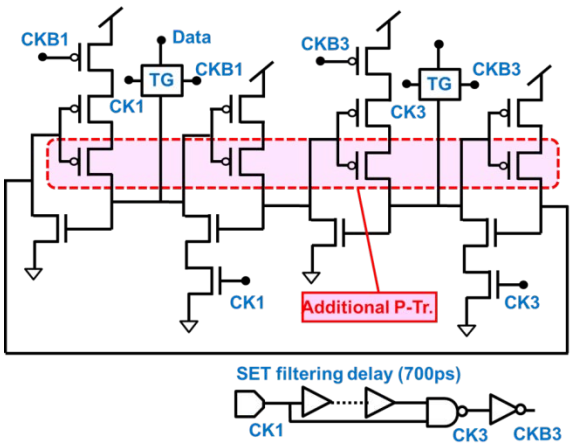


Fig.1. Schematic diagram of modified DICE.

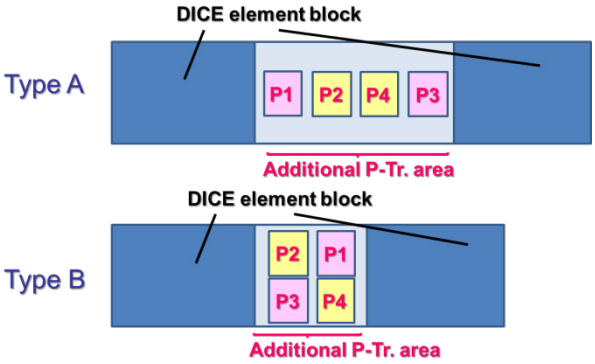


Fig.2. Outline of the circuit layout of modified DICE.

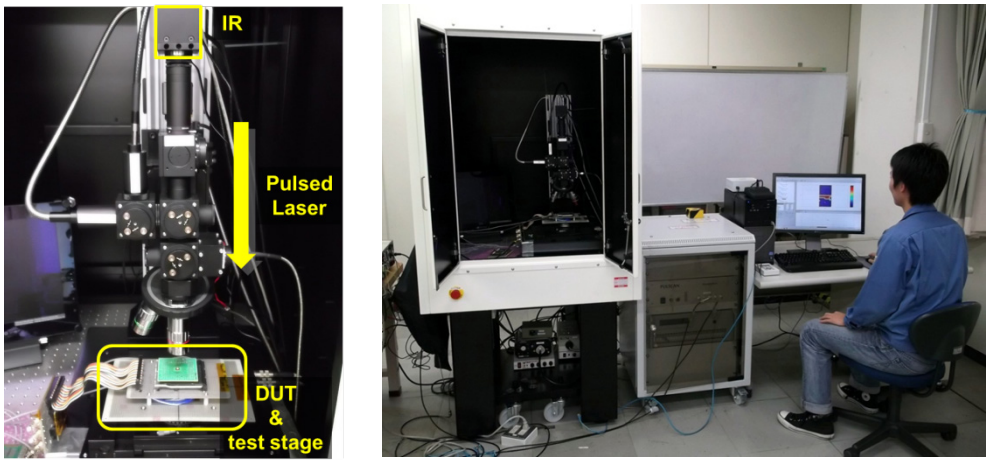


Fig.3. Pulsed-laser SEE test system. (@ JAXA Tsukuba Space Center.)

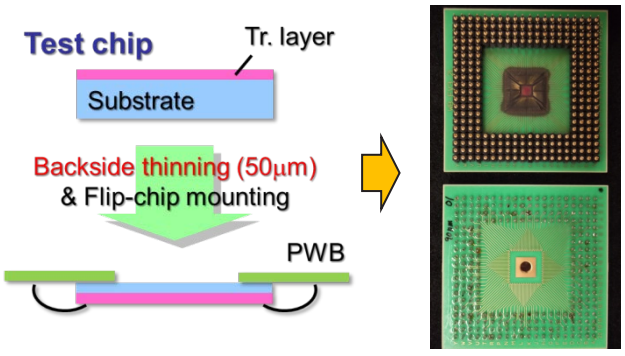


Fig.4. Procedure of the sample preparation used for the laser testing.

Table 1. Main profile of the pulsed-laser used in this study.

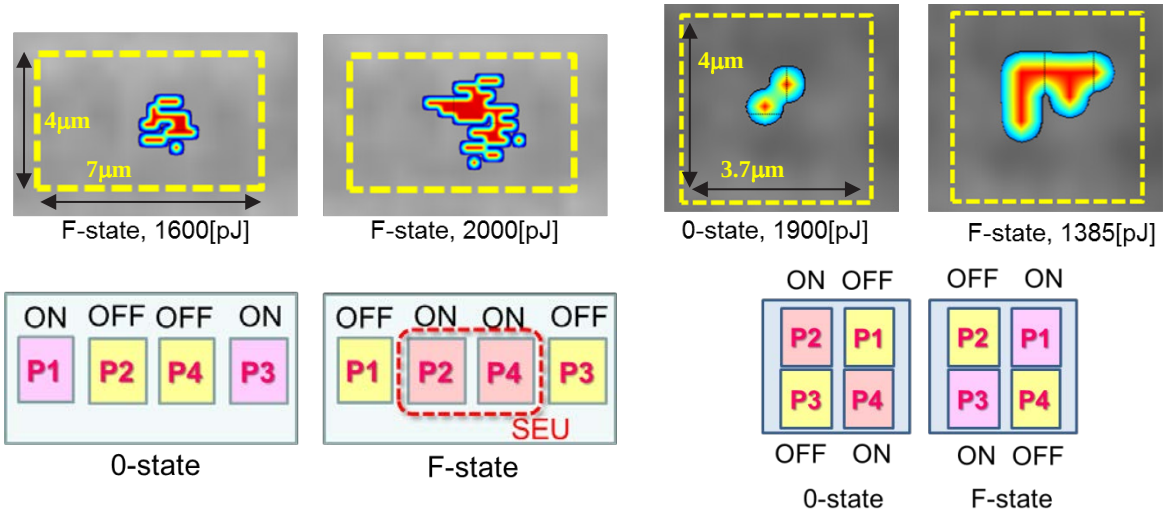
Parameters	Values
Laser Energy	up to 2,000 [pJ]
Wavelength	1,064 [nm]
Pulse duration	30 [ps]
Estimated spot diameter (@ $1/e^2$)	1.6 [μm]

3. Results and Discussion

At first the heavy ion irradiation was performed to check the SEE sensitivity of each test circuit. Specific Mono-energetic heavy ions were obtained from the Azimuthally Varying Frequency (AVF) cyclotron at Takasaki Radiation Chemistry Research Establishment of JAEA and the Heavy Ion Medical Accelerator synchrotron in Chiba (HIMAC), at the National Institute of Radiological Sciences (NIRS). As the result, unexpected SEUs were observed during the nomal angle (i.e. perpendicular to the chip surface) irradiation in addition to the angled irradiation test (Cross section characteristics are shown and discussed later compared with the pulsed-laser testing results.).

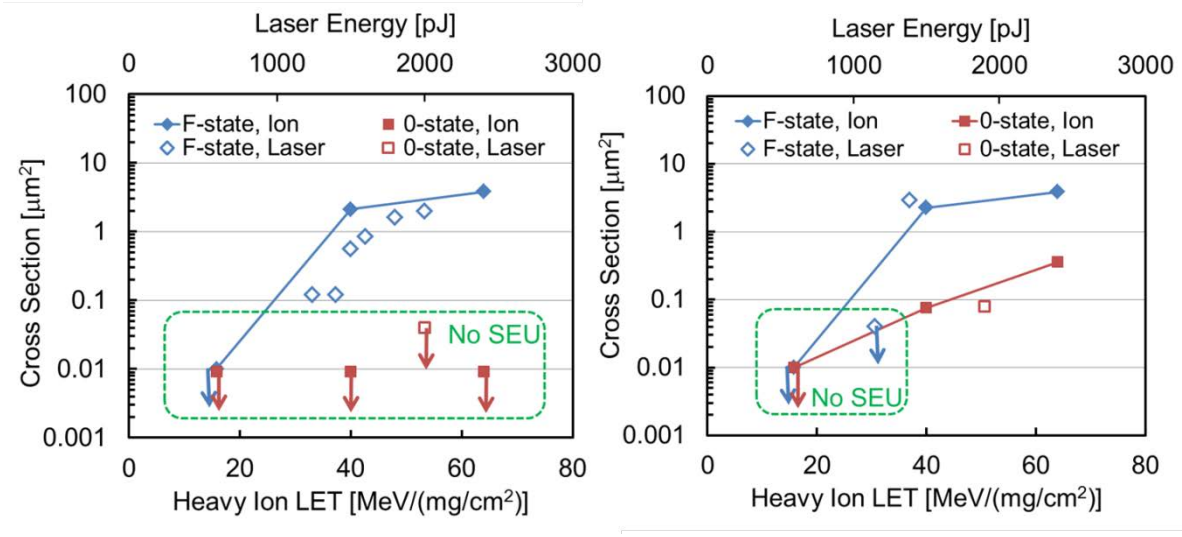
In order to clarify the location of sensitive nodes, pulsed-laser testing was performed. Fig.5 shows typical results of the error mapping obtained by the laser scanning. In the experiment of Type-A device, the error was observed only at F-state. This tendency agreed with the heavy ion irradiation test result previously mentioned. It was confirmed that the sensitive area was identified only in an additional P-Tr. area. It was also confirmed that the sensitive area was located on the center of an additional p-transistor area as shown in Fig.5(a). These facts suggest that SEUs were induced by a disturbance of electrical potential of a neighboring ON-state P-Tr. pair. With the Type-B device, SEUs were induced at both 0-state and F-state as shown in Fig.5(b). In this test case, memory cells were often permanently damaged during laser irradiation. It was thought that SEUs were induced by the same mechanism as Type-A device.

Cross section characteristics obtained by heavy ion irradiation and pulsed-laser test are shown in Fig. 6. Although further investigations about the relationship between the laser energy and the equivalent LET were needed, the cross-section determined from experiments showed good coincidence. Some investigations about the defining of a laser equivalent LET have already been reported[6-7]. Based on these studies it is roughly estimated that 100[pJ] (λ=1,064nm, sensitive volume depth d=1μm) is equivalent to the order of LET=10[MeV/(mg/cm^2)]. In case of our experiments, some elements which should be taken into consideration exist in calculating equivalent LET (For example, the limitation of the assumption of RPP model etc.). Additional experiments and numerical analysis are required to determine the laser equivalent LET in our test condition as the future work.



(a) Type-A (b) Type-B

Fig.5. Typical examples of the error mapping image obtained by the laser testing. The yellow dotted line shows additional p-transistor area described in Fig. 2.



(a) Type-A (b) Type-B

Fig.6. Cross section characteristics obtained by heavy ion irradiation and pulsed-laser tests.
(Note: The relationship between the upper horizontal axis and the lower one is not calibrated.)

4. Conclusion

This paper described the evaluation result of the SEE sensitivity of 90nm DICE based flip-flops. Pulsed laser testing methodology was successfully utilized to the identification of SEU sensitive nodes. However some restrictions also exist in the laser testing (For example, the laser is unsuitable for angle irradiation because of the limitation of the penetration depth). It is said that the evaluation which combined heavy ion irradiation test and the pulsed laser testing is very effective way for shortening a period required for an optimization of rad-hard circuit designs. Charge sharing issue becomes major concerns for nano-scale devices due to the scaling trends such as reduced nodal charge and reduced area spacing. Careful design layout that took the separation of the sensitive transistor pairs into account is required. Based on the result obtained in this study, we would like to accelerate the construction of the RHBD library corresponding to nanoscale devices for space applications.

Acknowledgments

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References

[1] A. Maru et al., "DICE-based flip-flop with SET pulse discriminator on a 90 nm bulk CMOS process," IEEE Trans. Nucl. Sci., vol. 57, pp. 3602-3608 (2010).
[2] A. Maru et al., "DICE based Flip-Flop with SET pulse discriminator on a 90 nm bulk CMOS process," Proceedings of 9th RASEDA, pp.64-67(2010).
[3] A. Amusan et al., " Charge Collection and Charge Sharing in a 130 nm CMOS Technology," IEEE Trans. Nucl. Sci., vol. 53, pp. 3253-3258 (2006).
[4] A. Amusan et al., " Single Event Upsets in Deep-Submicrometer Technologies Due to Charge Sharing," IEEE Trans. Device and Materials Reliability, vol. 8, pp. 582-589 (2008).
[5] B.D.Olson et al., " Simultaneous single event charge sharing and parasitic bipolar conduction in a highly-scaled SRAM design," IEEE Trans. Nucl. Sci., vol. 52, pp. 2132-2136 (2005).
[6] V.Pouget et al., " Theoretical investigation of an equivalent laser LET," Microelectronics Reliability, vol.41, pp. 1513-1518 (2001).
[7] D.McMorrow et al., " Application of a pulsed laser for evaluation and optimization of SEU-hard designs," IEEE Trans. Nucl. Sci., vol. 47, pp. 559-565 (2000).