SEE Tests of the 4Gb and 8Gb Nand Flash

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Abstract

This paper summarizes SEE test results on Micron 4Gb and Samsung 8Gb Nand Flash device focusing on High Current Events and Function Failure resulting from radiation events.

Introduction

NAND Flash uses floating-gate transistors, with the transistors connected in a structure resembling a NAND gate. Comparing to fault-free Nor Flash, Nand Flash also contains a limited number cell faults to maximize the storage capacity [1]. Both of these allow the Flash Nand to achieve very high density.
For space applications, many papers have been published on Nand Flash radiation characteristics. Most test results [2,3,5] show that Nand Flash is an acceptable solutionfor mass storage applications in space environments.
Meanwhile, as the process scaled down and the complicity of the control unit inside of the Nand Flash, some new phenomena, like High Current and Functional Failure, have been observed.
This paper characterizes Micron 4Gb and Samsung 8Gb Nand Flash SEE, not only SEL, SEU and SEFI but also High Current and Functional Failure. Moreover, this report is trying to summary an efficient test method to characterize different Single Event Effects and calculate their rates.

Description of Devices Under Test(DUT)

The tests performed at Catholic University of Louvain on May and December, 2011 and March 2012. Approximately forty delidded samples from Micron and Samsung were irradiated.

Table 1: SEE tests samples summary

Manufacture	Type	Density	Package	LDC	Sample Size
Micron	Nand SLC	4Gb	SOP48	1006	19
Samsung	Nand SLC	8Gb	SOP48	1031 1004	16

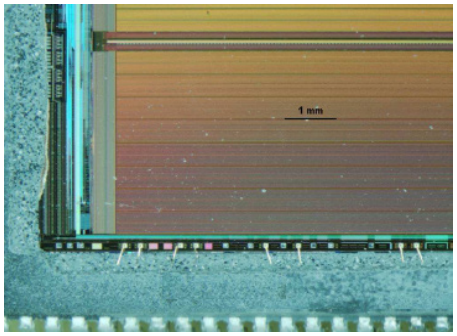

Figure1: Samsung 8GbNand Die

Experimental Procedure

Test facility: Catholic University of Louvain Cyclotron (U.C.L).

Table 2 Describes the availableions for the heavy ion SEE testing.
During the test, the power supply is monitored by a Protection circuit with a current threshold limiter. When an event occurs, the Protection circuit sends a trigger command to the oscilloscope to record this one, holds on the power supply during 1ms and cuts off during 7ms. Then, the power supply is applied again with the expected nominal current consumption. During the test current consumption is recorded with an ammeter at a sampling rate of one record every 150ms, and plotted for each run.
We performed runs up to a fluenceof 1.10^6 particles/cm^2

Table2 : Ions/Energys and LETs/Ranges

	Ion	DUT energy [MeV]	Range [µm Si]	LET [MeV/mg/cm²]
FORT LET	$^{124}Xe^{26+}$	420	37	67.7
	$^{84}Kr^{17+}$	305	39	40.4
	$^{40}Ar^{8+}$	151	40	15,9
	$^{20}Ne^{4+}$	78	45	6.4
	$^{15}N^{3+}$	60	59	3.3
FORT RANGE	$^{83}Kr^{25+}$	756	92	32,6
	$^{58}Ni^{18+}$	567	100	20.4
	$^{40}Ar^{12+}$	372	117	10,2
	$^{22}Ne^{7+}$	235	216	3
	$^{13}C4+^{+}$	131	292	1.1

for SEU, MBU, SEFI, while a fluence of 1.10^7 particles/cm^2 for the SEL, Functional Failureand High Current Events. During SEU, MBU and SEFI tests, a latchup monitoring was also done on the component's power supply in conjunction with the Protection circuit to eliminate destructive latchups.

Three test modes have been used:

- Static biased : SEL, SEU, MBU, SEFI, HCE, FF
- Dynamic Read Only: SEU, MBU, SEFI, HCE, FF
- Dynamic Erase/Write: SEU, MBU, SEFI, FF

* HCE: High Current Event, FF: Functional Failure

Current Threshold settings:

- SEL testing: High Current threshold guard to identify Real SEL form High Current Event;
- High Current Event (Standby + dynamic mode during irradiation): Low Current threshold guard to count the High Current trigger during irradiation, and also power cycle after the triggers;
- Functional Failure (Dynamic Read-only + Read-Write during irradiation): No current guard to identify all possible events, and also functional verification continually till events.

Results

1. SEL

No SEL observed for both Micron 4Gb and Samsung 8Gb samples during the tests until 67.7Mev.cm^2.mg^{-1} at 125C degree Static mode.

2. SEU, MBU & SEFI

SEUs and MBUs are defined by nondestructive single (SEU) or multiple (MBU) changes in the cell logic state from one to zero or vice-versa, and for which the cell logic state can be rewritten or reset. A SEFI is defined as a component state exhibiting a locked behavior requiring a complete reset of the system; in the context of this test, a SEFI is considered to be: at least half of a page of the flash memory exhibiting errors, or operational timeouts (the component performs operations with a period greater than device specifications).
Figure2 to Figure7 show the results from the tests in different test modes.

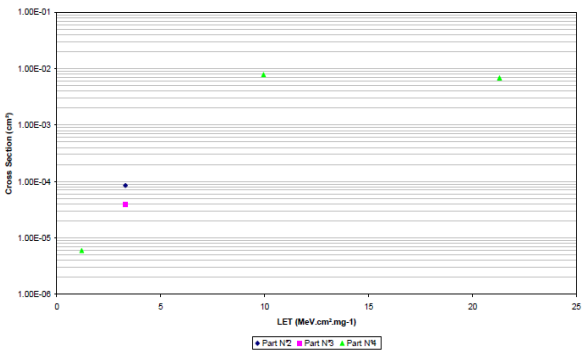

Figure 2: SEU Full static Mode cross section, Micron 4Gb Flash

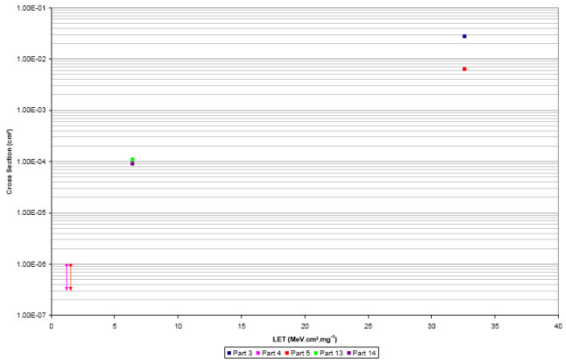

Figure 3: SEU Full static Mode cross section, Samsung 8Gb Flash

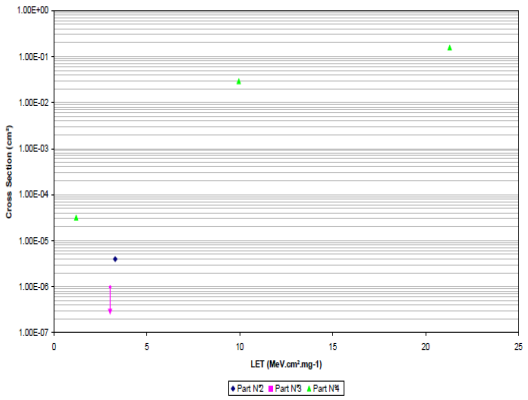

Figure 4: MBU Read only Mode cross section, Micron 4Gb Flash

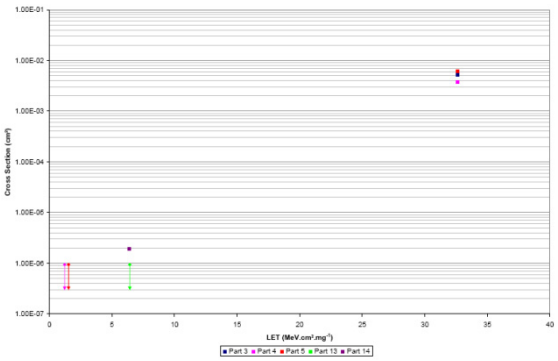

Figure 5: MBU Read only Mode cross section, Samsung 8Gb Flash

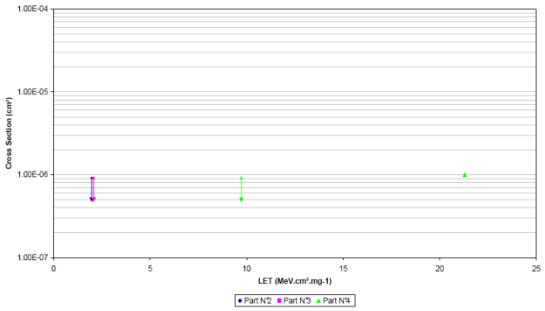

Figure 6: SEFI Erase/Write Mode cross section, Micron 4Gb

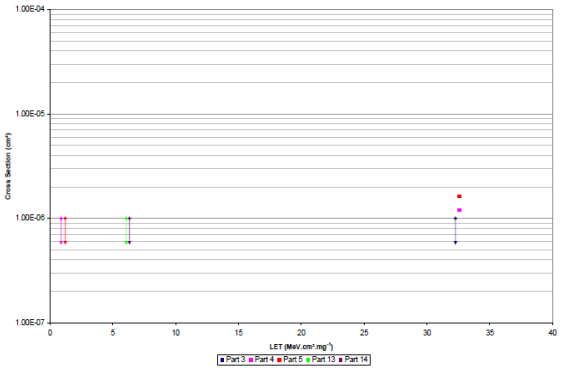

Figure 7: SEFI Read only Mode cross section, Samsung 8Gb

3. High Current Event

High Current Events, or High Current Spikes, have been observed and mentioned in previous studies [2,3,5], and researched in study [2] with a description of the High Current mechanism in study [4].

During our SEE testing, High Current Events observed from both Micron and Samsung, and the Micron current curve exhibited a much higher current peak. Figures 8 and 9 are examples of 4Gb Micron Nand Flash current curves during SEL (High Current threshold) and High Current Eventtest (low current threshold).

Although much higher current peak was recorded during Micron 4Gb Nand Flash test, no Functional Failure was found.

To evaluate the risk, we set 50mA as the current threshold to measure the High Current Event, and the results show in Table 3.

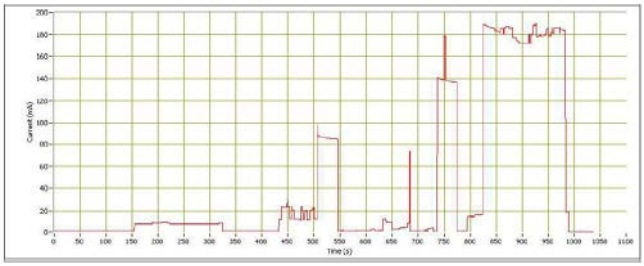

Figure 8: Current curve during SEL testing (no trigger) at LET=40.1Mev.cm^2.mg^{-1}

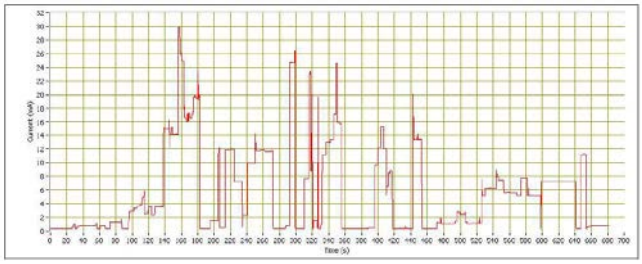

Figure 9: Current curve during High Current testing (low current threshold, triggers) with LET=40.1Mev.cm2.mg-1

Table3: Micron 4Gb HCE triggers Crosse Section

LET Eff [MeV/mg/cm²]	Cross Section (cm2)
40.1	6.00E-07
31	2.00E-07
21.3	2.00E-07

4. Functional Failure

During Samsung 8Gb SEL test, no SEL event was observed, and the current peak was much lower than Micron 4Gb, but some Functional Failures were observed in functional verification at High LET.

Additional tests with a fluenceof 1.10^6 particles/cm^2 have been performed at 25C degree for Read only mode and 125C degree for Erase/Write Mode, results are summarized in table4.

Only one fail at LET=59.86 MeV/mg/cm² has been observed at the end of the irradiation with the fluenceapproaching 1.10^6 particles/cm^2.

Table 4: Samsung 8Gb Functional Failure test result

LET Eff [MeV/mg/cm²]	Functional Mode During Irradiation					
	Read Only			Erase/Write		
	No2	No3	No 4	No2	No3	No 4
59.86	X	Pass	Fail	X	Pass	X
32.6	Pass	Pass	X	X	Pass	Pass
10.2	Pass	Pass	X	Pass	Pass	X

Discussion

There were very few surprises during SEU&SEFI tests, and the test results in general corresponded to previous studies. The approximate error rate calculated in an Adams 90 GEO orbit Environment for each component is summarized as follows:
Micron 4Gb Nand Flash Single bit Upset rate: 6.56E-15 error/bit/day, and SEFI rate: 3.1error/device/year;
Samsung 8Gb Nand Flash Single bit Upset rate: 3.46E-16 error/bit/day, and SEFI rate: 0.1error/device/year.
The data provided by the Die manufactures show that Micron 4Gb and Samsung 8Gb samples have similar Estimated Failure Rate (FIT), around 5 failure per 109 hours. From the High Current Event and Functional Failure results in the former chapter, we may calculate that the event rates are the same order of the FITin an Adams 90 GEO orbit Environment around 3 to 4E-3 error/device/10years.

However, the High Current Event and Functional Failure mechanisms may disturb the SEL test because the current threshold setting and Functional verification are sensitive in determining an SEL event.
As mentioned in this report, Micron 4Gb had much higher peak current but without Functional Failure comparing that Samsung 8Gb had Functional Failure but it did not show direct link to the current. In this case, the current threshold setting is critical.
After several evaluations, we set the current threshold at high level during SEL testing, and a relative low level during High Current Event testing with no threshold during Functional Failure testing. During testing nominal currents were variable between components, which make it difficult to establish a uniform definition of the current thresholds for each level which is supported by observations during testing and prior studies. We also did not see the direct link between the High Current Event and the test modes.
We noted that another factor impacted the accuracy of the result is the flux. To accelerate the test, normally the tester takes higher flux, which increases the risk of two particles striking at one transistor at a time. However in space, the ions flux is so low, it will be never happen. Meanwhile, the ground test result probably will completely change at same fluence but with lower flux.

Conclusion

We measured the Micron 4Gb and Samsung 8Gb SEE characteristics. Complex designs and small feature sizes of the Nand Flash samples in conjunction with High Current Events, Functional Failures and the flux complicated the test results and analysis.

After improvements in measurement procedures we established a comprehensive characterization routine for SEL, SEU, MBU, SEFI, High Current Event and Functional Failure testing and analysis. The results indicate the Micron 4Gb and Samsung 8Gb Nand Flash are ideal components for most of the space missions. In our evaluation new events were observed in High Current and Functional Failure areas, but the rates are very low (Same level of FIT as showed in previous chapter).

In summary this report has documented test methods and test results of Nand Flash SEE, including new events, and characterizes them in space environment.

References

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