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Evaluation of Cryogenic Readout Circuits with GaAs JFETs for Far-Infrared Detectors

By

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Abstract: The characteristics of gallium arsenide junction field-effect transistors (GaAs JFETs) and the performance of cryogenic readout circuits using GaAs JFETs for two-dimensional far-infrared arrays are evaluated at cryogenic temperature. We fabricated the GaAs JFETs with various gate sizes ranging from W/L = 5μm/0.5μm to 200μm/200μm to systematically measure their static characteristics and low-frequency noise spectra. We found that the low-frequency noise voltage depends on the device size in the saturation region of GaAs JFETs at 4.2 K, and the power density of the noise voltage is inversely proportional to the gate area. These findings allowed us to determine the Hooge parameter of the GaAs JFET at 4.2 K to be 4×10^{-5}, assuming that the carrier mobility is 1.5×10^{3} cm^2/Vs. On the other hand, we did not find the obvious correlation between the low-frequency noise and gate size in the ohmic region of GaAs JFETs. Based on these measurements for GaAs JFETs, we fabricated and tested a dual GaAs JFET, a source-follower-per-detector (SFD) circuit, and a 20$\times$3 channel SFD circuit array. The Common-Mode-Rejection-Ratio (CMRR) of the dual GaAs JFET with W/L = 50μm/20μm at 4.2 K was determined to be 40–60 dB under small power dissipation. The performance of SFD circuits and the 20$\times$3 channel SFD arrays for two-dimensional far-infrared Ge:Ga detector readouts are currently being evaluated.

1. INTRODUCTION

In the far-infrared (FIR) wavelength region, FIR imaging devices are planned to be used instruments on board the future space astronomical satellite missions, such as the Japanese HII/L2 mission scheduled for launch in 2010 (Nakagawa et al. 1998), and for non-destructive imaging inspection of various objects. Gallium-doped germanium (Ge:Ga) photoconductors, which are the most sensitive detector in the FIR region between 60 and 200 μm, and for wavelengths longer than 200 μm bolometers are utilized as detector elements in FIR imaging devices. These FIR detectors are usually operated below 4 K to obtain a high sensitivity and to decrease the dark current. Thus, their readout electronics must also work at cryogenic temperature. Therefore, cryogenic field-effect transistors (FETs) are critical elements to building the FIR imaging device system.

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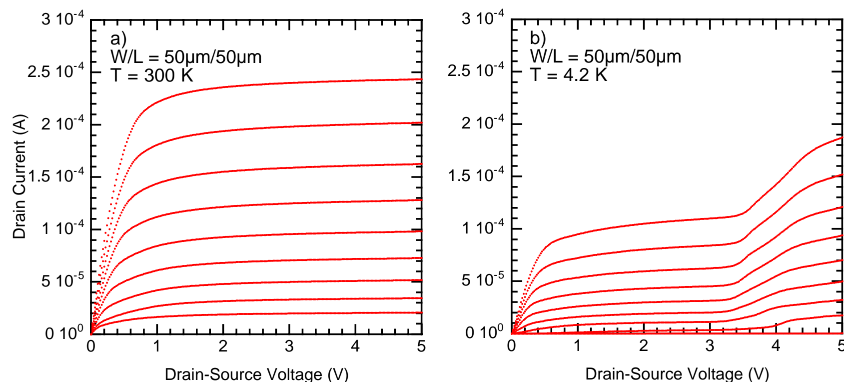

Fig. 1: Example of the DC characteristics of n-channel GaAs JFETs with W/L = 50μm/50μm at (a) 300 K and (b) 4.2 K. Curves in both figures correspond to the drain-source currents at gate-source voltages from 0.2 to 0.6 V in step of 0.1 V.

Cryogenic FETs must satisfy the following requirements: (1) Since the FIR detectors are usually used below liquid-helium temperature, FETs must operate at the same temperature as the detectors. (2) The low-frequency noise voltage of FETs must be less than that of FIR detectors. Therefore, it is necessary for imaging arrays using Ge:Ga photoconductors to have a noise voltage below 1 μV/Hz$^{1/2}$ at 1 Hz at the operating temperature. (3) High input impedance and small-input capacitance are required for making cryogenic readout circuits. (4) In order to prevent the detector arrays from becoming warm, cryogenic FETs need to operate with low power dissipation. This is especially important for space applications in which the volume of the refrigerants that can be carried and the cooling power of mechanical coolers are limited.

As a result of investigations into the performance of several types of FETs at cryogenic temperature (Kirschman 1993), silicon MOS-FETs and GaAs JFETs are presently being used for the cryogenic readout. In particular, these investigations have led to advancements in the development of cryogenic readouts with Si MOS-FETs, which can be applied to the existing Si CMOS technology (Young et al. 1998; Noda et al. 1998). They have already been used in the ISO mission (Kessler et al. 1996) and, moreover, will be adopted to the far-infrared detector arrays of the SIRTF mission (Fanson et al. 1998) scheduled for launch in 2001 and the FIS (Far-Infrared Surveyor) instrument on the Japanese infrared mission (ASTRO-F) in 2004 (Murakami et al. 1998).

Developments in cryogenic readout electronics using GaAs JFETs have also been advanced by several groups (Goebel et al. 1992; Cunningham & Fitzsimmons 1998; Okumura et al. 1998). Measurements have indicated that GaAs JFETs have good static characteristics and low noise performance at cryogenic temperature. A CRL group has also developed GaAs JFETs for far-infrared imaging devices using unstressed and stressed Ge:Ga photoconductors over the past several years. In this paper, we describe the characteristics of n-type GaAs JFETs and show experimental results for several types of cryogenic circuits with GaAs JFETs at cryogenic temperature.

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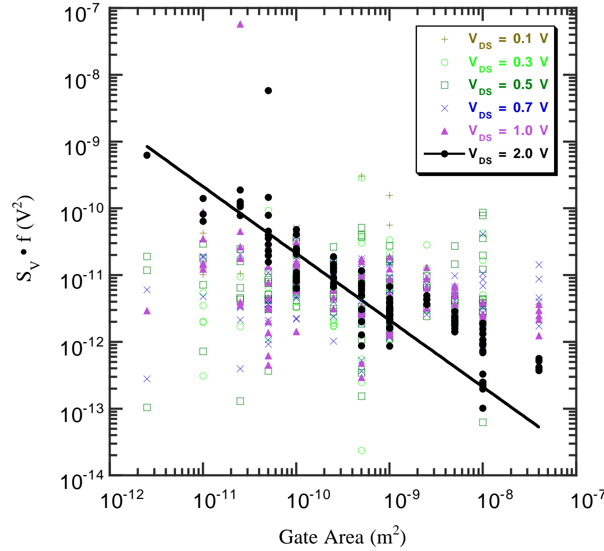

Fig. 2: Plot of the noise voltage as a function of the gate area. The various symbols show the data for different drain-source voltages at 0.1, 0.3, 0.5, 0.7, 1.0, and 2.0 V. The solid line indicates the function $S_V \cdot f = K_f/(\text{gate area})$, where $K_f = 2000\ \mu V^2\ \mu m^2$ at $V_{DS} = 2.0$ V.

2. DC AND NOISE CHARACTERISTICS

The n-channel GaAs JFETs of D-modes and E-modes were fabricated by the SONY Corporation. To investigate the dependence of their DC and noise performance on their gate size, we tested them with gate sizes ranging in gate width from 2 to 200 μm and in gate lengths from 0.5 to 200 μm.

Figure 1 shows the DC characteristics of the GaAs JFET with W/L = 50μm/50μm at 300 and 4.2 K. Samples of the GaAs JFET with other gate sizes were found to have similar DC characteristics at 300 and 4.2 K. The drain-source currents (I_{DS}) at 4.2 K decreased to about 40% of those at 300 K when the drain-source (V_{DS}) and gate-source (V_{GS}) voltage conditions were the same. This is because the threshold voltages of GaAs JFETs changed by approximately +0.4 V as the temperature drops from 300 to 4.2 K. The transconductance (gm) of this GaAs JFET was about 80 μS at 4.2 K for the drain-source current of 10 μA.

Table 1: Typical noise characteristics of GaAs JFETs at 4.2 K.

Gate Width: Wg	Gate Length: Lg	V_{DS}	I_{DS}	Power Dissipation	gm	input-referred noise voltage	S_I
(μm)	(μm)	(V)	(μA)	(μW)	(μS)	(μV/ $Hz^{1/2}$)	(A^2)
10	5	0.5	13	6.4	133	2.9	1.5×10^{-19}
100	100	2	25	50	114	1.0	1.4×10^{-20}
5	200	2	1.4	2.8	4.7	1.6	5.6×10^{-23}
200	200	2	20	40	93	0.75	4.8×10^{-21}

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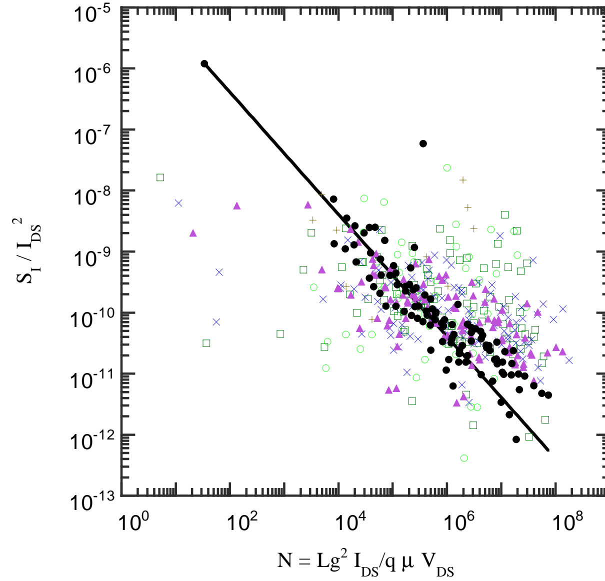

Fig. 3: Plot of the normalized power-density of current noise ($S_I/{I_{DS}}^2$) against the number of carriers (N). Symbols are the same as in Figure 2. The solid line shows the Hooge law with a Hooge parameter (α_H) of 4×10^{-5}.

The reduction of low-frequency noise is important because cryogenic readout circuits for infrared detectors are typically operated in frequency ranges below 1 MHz. A 1/f-noise component is generally dominant in the low-frequency noise of JFETs. The 1/f-noise voltage is inversely proportional to the gate area of JFETs (Kirschman, Lemoff, & Lipa 1992). However, the dependence on the V_{DS} and V_{GS} on the 1/f-noise is not clear. Therefore, we systematically investigated the relationships between the 1/f-noise component and the characteristics of GaAs JFETs (V_{DS}, V_{GS}, and gate size).

Dominant 1/f-noise components were observed for all measured noise spectra of GaAs JFETs. Under several measured conditions, Lorentz-shaped generation-recombination (g-r) noise components were superimposed on a 1/f-noise spectrum in the low frequency region. In those cases, we extracted the 1/f-noise components from the measured noise spectra. The typical input-referred 1/f-noise voltages are shown in Table 1.

Figure 2 plots the input-referred power density of voltage noise (S_V) against the gate size of GaAs JFETs at 4.2 K. The data were obtained for V_{DS} from 0.1 to 2.0 V, and for V_{GS} from 0.2 to 0.6 V. In the saturation region of the GaAs JFET ($V_{DS} > 1$ V), the power density of noise voltage is inversely proportional to the gate area. This result is consistent with the findings of Kirschman et al. (1992). The coefficient of the inverse correlation, K_f ($= S_V\cdot$ frequency $\cdot$ gate area), is about 2000 $\mu V^2 \mu m^2$ for $V_{DS} > 1.0$ V. On the other hand, in the ohmic region for $V_{DS} < 0.5$V, the noise power density of voltage noise does not change with the gate area, and greatly varies depending on V_{DS} and V_{GS} conditions.

For 1/f-noise in semiconductor materials, an experimental law was deduced by Hooge (1969): $S_I/I^2 = \alpha_H/f \cdot N$, where S_I is the spectral density of the current noise that is determined to be $S_I = gm^2 S_V$, f is the frequency, N is the total number of free carriers contributing to the generation of 1/f-noise, and α_H is the Hooge parameter which is assumed to be constant.

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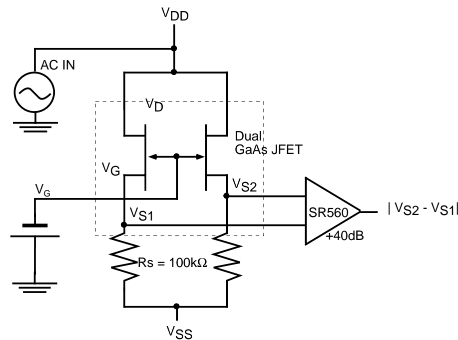

Fig. 4: Measurement circuits of the CMRR in Dual GaAs JFETs.

Assuming that the GaAs JFET has a homogeneous electric field in a homogeneous channel, the number of free carriers in the channel is estimated to be $N = Lg^2 I_{DS}/q\mu V_{DS}$, where Lg is the gate length, q is the electron charge, and μ is the carrier mobility. Figure 3 plots the S_I/I^2 against the number of free carriers, which was calculated using device parameters. Here, we take the mobility of the carriers to be the Hall mobility of $\mu = 1.5 \times 10^3$ cm^2/Vs, which is estimated by the Hall measurements of GaAs samples having the same structure as GaAs JFETs at 4.2 K. An inverse correlation is clearly observed in the saturation region at $V_{DS} >$ 1 V, which is shown in the figure 3. From this correlation, we obtain the Hooge parameter of the GaAs JFET as $\alpha_H = 4 \times 10^{-5}$ at 4.2 K.

It is suggested that 1/f-noise is the fluctuation in the mobility of carriers with a 1/f spectrum (Hooge 1994). The dependence of Hooge parameters on the mobility of carriers was also measured, and it was found that the mobility is due to several different mechanisms resulting from the carrier interactions. Two scattering mechanisms, phonon scattering and impurity scattering, were the main contributors to the mobility. At cryogenic temperature, impurity scattering tends to be the main mechanism for the carrier scattering. The contribution of the phonon scattering to the Hooge parameter was estimated by the Ziel model (van der Ziel et al. 1985), but that estimate at 4.2 K is much smaller than that obtained by our measurements for GaAs JFETs. We therefore believe that the α_H is determined by the contribution of impurity scattering.

In the ohmic region of the JFETs, however, the results shown in figure 3 are not consistent with the Hooge law. Detailed analysis is necessary to consider the influence of series resistance on the channel of the GaAs JFET, the uncertainty surrounding the estimation of the total number of carriers, and the change in Hooge parameter with bias voltages.

3. PERFORMANCE OF CRYOGENIC DUAL JFETS

Dual FETs are important in a wide range of precision applications used to amplify the voltage difference between two input signals. They are often used as the differential amplifier of readout circuits for infrared detectors because they can subtract a common-mode noise from weak signals. For this application, they need to have a high Common Mode Rejection Ratio (CMRR), which is the ratio of response for normal-mode signals to that for common-mode signals, and small differential voltage in the case of two of the same input voltages at cryogenic temperature.

We fabricated the monolithic n-channel GaAs JFET Duals using the same technique used

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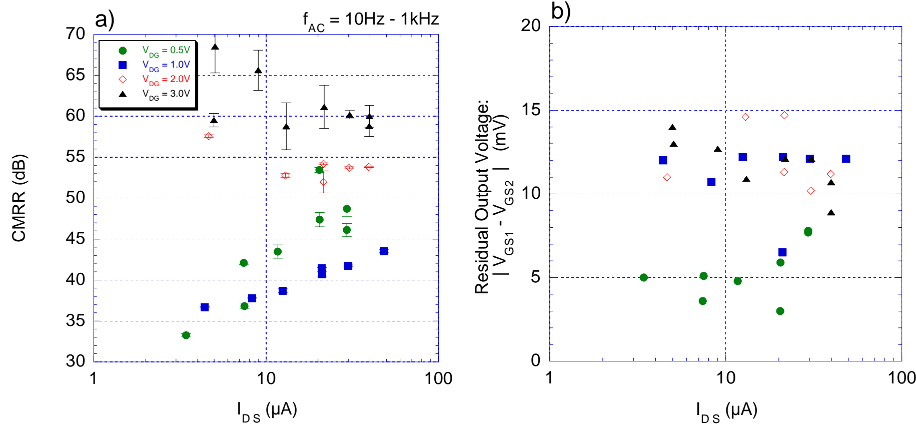

Fig. 5: Cryogenic performance of the dual GaAs JFET with W/L = 50μm/20μm at 4.2 K. (a) The CMRR and (b) the residual output voltage as a function of the drain-source currents.

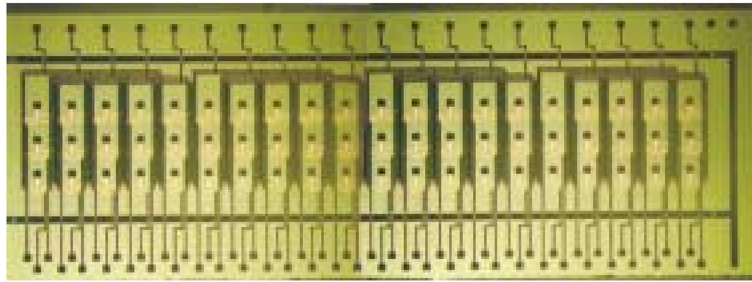

Fig. 6: Photograph of the 20×3 channel SFD array using GaAs JFETs.

for discrete GaAs JFETs. The DC characteristics and noise performance at 300 and 4.2 K are consistent with those found previously for discrete GaAs JFETs. Figure 4 shows circuits used for the measurement of the CMRR and the residual output voltage of dual GaAs JFETs. The source resistance is exactly 100 kΩ. The CMRR of the circuit was about 90 dB. From the measurements, the CMRR is determined from the formula: $CMRR = 20log\Delta V_{DG}/\Delta|V_{GS1} - V_{GS2}|$, where V_{DG} is the drain-gate voltage, and V_{GS1} and V_{GS2} are the gate-source voltages of each GaAs JFET.

The results for each drain-gate voltage are shown in Figure 5. The symbols indicate the different drain-gate voltages, where V_{DG} = 0.5, 1.0, 2.0, and 3.0 V. The CMRR of the dual GaAs JFETs with W/L = 50μm/20μm at 4.2 K is about 40 dB under small power dissipation ($< 10\ \mu$W). Under ordinary power condition (about 100 μW), it was found to be more than 60 dB. The differential output voltages were less than 15 mV at 4.2 K in the range of I_{DS} = 10–100 μA. The differential output voltages are generally the same as those of the dual Si JFET at room temperature. Moreover, it was found that the change in the CMRR and offset voltages between 300 and 4.2 K was very small. Therefore, we conclude that the dual GaAs JFETs are beneficial because of their high CMRR and low offset voltage of output signals at cryogenic temperature. We plan to broaden the applications of the dual JFETs for the readout

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of the single infrared detector to include such elements as an impedance transfer circuit for TIA and an input circuit for a cryogenic operational amplifier.

4. READOUT FOR FIR ARRAY

To test the fabrication of a cryogenic operational amplifier for CTIA readout, one source-follower-per-detector (SFD) circuit using GaAs JFETs was fabricated on a chip. In addition, chips for a 20×3 channel SFD readout using GaAs JFETs, which has a format similar to that of the Si MOS-FET readout of FIR instruments on the Japanese Astro-F satellite, were also manufactured for use in the building of a system for a Ge:Ga FIR photoconductor two-dimensional direct hybrid array (Fujiwara et al. 1999). A photograph is presented in Figure 6. We are currently evaluating their fundamental performance and making various tests of these readouts at 4.2 K. Preliminary results from these measurements show that the SFD circuits perform well.

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