Dual-PLL based on Temporal Redundancy for Radiation-Hardening

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Abstract

This paper proposes a dual-PLL based on temporal redundancy for radiation-hardening. A common practice technique for radiation-hardening is the triple modular redundancy (TMR). However, it is inefficient to apply for PLLs because PLLs include huge size of capacitance and static current consumers, means analog circuits. Thus, we propose a dual-PLL and a detective circuit that detects a perturbed PLL by radiation-strike. Although our proposal is based on DMR, it allows both detecting and correcting the clock-perturbation. The detective circuit based on temporal redundancy switches a clock-path from one perturbed PLL to the other PLL. In radiation-simulation, 88.4% of cycle-to-cycle jitter is suppressed.

1. Introduction

Phase-locked loops (PLLs) in digital circuits are source of the clock signal. Perturbation on PLLs is a crucial because change or lack of clock signal leads whole system malfunction. Single-event (SE) is considered as one of the causes of PLL malfunctioning. Thus, importance of radiation-hardened PLL is increasing.

Fig. 1 shows block diagram and microphotograph of unhardened PLL. The unhardened PLL consists of both digital sub-circuits such as the divider and phase frequency detector (PFD) and analog sub-circuits such as the charge-pump (CP), loop filter (LF) and voltage controlled oscillator (VCO). The CP and VCO are static current consumers and the capacitors in LF consume large silicon area as shown in the microphotograph. Therefore, the triple modular redundancy (TMR) is inefficient for PLLs because PLLs includes the huge size of capacitance and static current consumers, means analog circuits.

To mitigate penalties of the TMR in power and silicon area consumption, some studies applied TMR for the VCO and digital sub-circuits [1], [2]. Even though this strategy improves radiation-hardening in PLLs, other analog sub-circuits that cannot apply the TMR are out of protection. For the unprotected analog sub-circuits, circuit-design has to be changed in order to harden radiation-strike. One example is that the current-mode CP is replaced by the voltage-mode CP [3]. Nevertheless, changing circuit-design leads to degradation in performance of PLLs such as the jitter. Consequently, designers must optimize trade-off between these penalties and radiation-hardening.

This paper proposes a dual-PLL based on temporal redundancy for radiation-hardening. The proposed radiation-hardened PLL (RHPLL) utilizes dual modular redundancy (DMR) with a detective circuit. Although the proposed RHPLL is DMR, the detective circuit enables not only detecting but also correcting clock-perturbation. The detective circuit based on temporal redundancy switches a clock-path, which goes to digital circuits, from one perturbed PLL to the other PLL. Since the RHPLL is based on the DMR technique, the power and silicon area is smaller than TMR. Furthermore, all sub-circuits are in protection without degradation of performance. For the simulation of radiation-strike, the proposed RHPLL designed by TSMC 0.18um achieves 88.4% of cycle-to-cycle jitter improvement, which is from 1588ps to 184ps, in 2.5ns normal clock period.

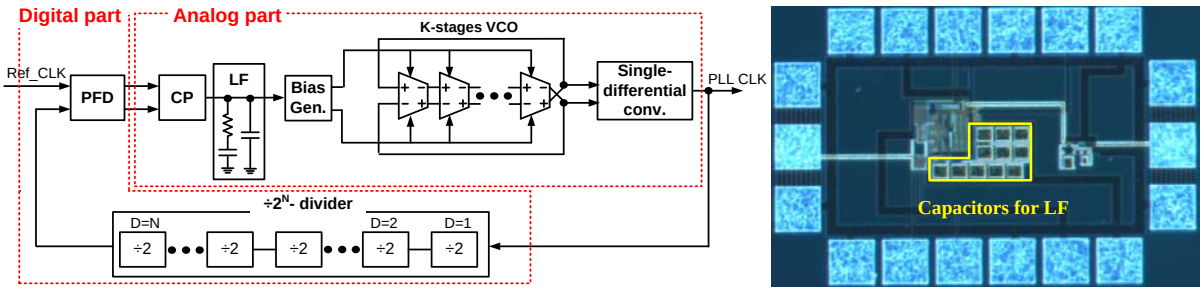


Fig. 9. Block diagram and microphotograph of an unhardened PLL.

2. Proposed Radiation-Hardened PLL

2.1 Basic concept: dual-PLL and detective circuit

The proposed RHPLL consists of dual-PLL and one detective circuit. If one of two PLLs has clock-perturbation by radiation-strike, the detective circuit detects the PLL that has clock-perturbation. Then, it switches the clock-path from the detected PLL to the other PLL. The clock that goes to digital systems is called 'final clock' in this work. Fig. 2 shows the basic concept of the dual-PLL and detective circuit.

Unlike TMR, use of DMR has an issue that distinguishes between perturbed clock and non-perturbed clock. In case of TMR, it is easy to distinguish non-perturbed clock because identical two of three clocks is definitely the non-perturbed clock. In contrast, DMR can only recognize that clock-perturbation occurs but cannot distinguish which PLL has clock-perturbation. To overcome this issue in DMR, we utilize temporal redundancy for the detective circuit.

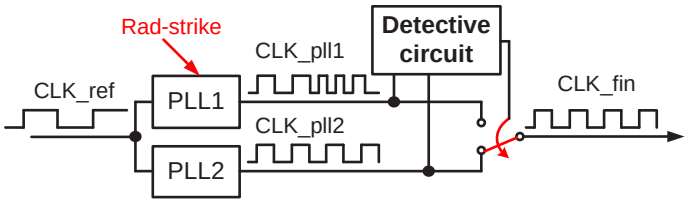
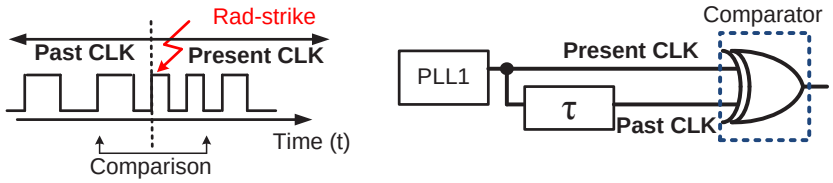


Fig. 10. Basic concept of the dual-PLL and detective circuit.

2.2 Detective circuit based on temporal redundancy

The key idea to distinguish perturbed and non-perturbed clocks is comparison of clocks between before and after radiation-strike at each PLL output. The constant periods of PLL clocks are changed after radiation-strike as shown in Fig. 3 (a). Hence, if the clock before radiation-strike (past clock) and the clock after radiation-strike (present clock) are different in a PLL, it means the PLL has clock-perturbation. On the other hand, if the past and present clocks are identical, the PLL is in normal operation. To generate the past clocks, delay-lines that generate one-period delayed clocks are used in this work. The past and present clocks are compared by an XOR-gate in order to check whether they are identical or not as shown in Fig. 3 (b). Due to this detective circuit based on temporal redundancy, the proposed RHPLL enables to both detect and correct clock-perturbation unlike the conventional DMR technique.

Fig. 4 shows waveforms when radiation-strike occurs on one side of PLL. While the past clock emits clock-perturbation after one period of radiation-strike, the present clock emits the clock-perturbation as soon as radiation-strike occurs. The difference between the past and present clocks produces a perturbation-detecting signal at the output of XOR-gate. Based on the perturbation-detecting signal, the detective circuit selects one the final clock.



(a) (b)

Fig. 11. (a) The key idea to distinguish perturbed and non-perturbed clocks (b) detective circuit based on temporal redundancy

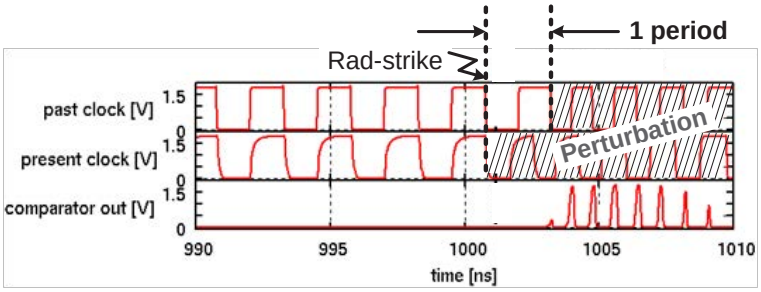


Fig. 12. Production of perturbation-detecting signal at the output of XOR-gate

2.3 Implementation

The delay-line for the detective circuit should be carefully implemented to ensure exact 'one period' clock delay because deviation of phase leads to a perturbation-detecting signal even without radiation-strike. To implement perfect one period delay, unit-cells for the delay-lines are identical with those used for VCOs. The unit-cells need two bias voltages for NMOS tail current sources (Vbn) and PMOS active-load (Vbp) as shown in Fig. 5 (a). There are two requirements for these bias voltages in the detective circuit design. Firstly, in non-perturbation, the bias voltages for the delay-line must be identical with those for VCOs in order to ensure 'one period' clock delay. Secondly, in perturbation, the delay-lines must have different bias voltages from perturbed bias voltages of VCOs. If the bias voltages for delay-lines are identical with the perturbed bias voltages of VCOs, the detective circuit cannot detect perturbation as shown in Fig. 5 (b).

As the solution of the requirements, the bias voltages for the delay-lines are generated by taking average of two VCO bias voltages with a pair of resistors as shown in Fig. 6. In non-perturbation, the bias voltages for the delay-lines (Vbn_d, Vbp_d) are identical with those of VCOs because the two VCO bias voltages are identical. However, if one VCO bias voltage is changed by radiation-strike, Vbn_d and Vbp_d have averaged value between the changed and normal VCO bias voltages. Thus, this solution satisfies those two requirements.

Fig. 7 shows the full structure of the proposed RHPLL. Each perturbation-detecting signal goes out from the XOR-gates and then is driven as inputs of SR-latch. The SR-latch generates control signal for switching of MUX. If PLL1 has clock-perturbation, the final clock becomes PLL2's clock through switching of the SR-latch. During non-perturbation in both PLLs, the SR-latch keep previous control signal.

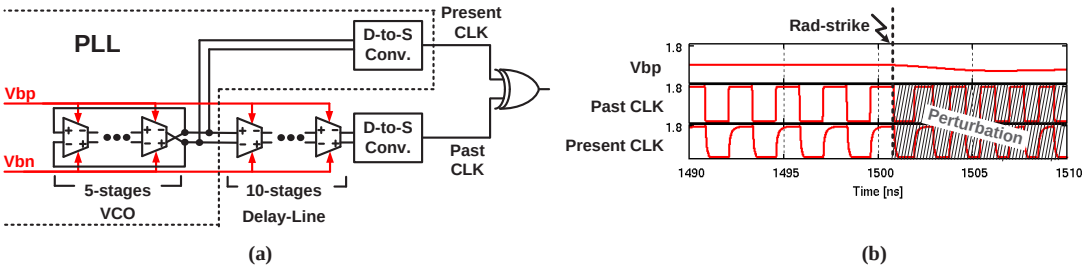


Fig. 13. Bias voltages issue in implementation of the delay-lines.

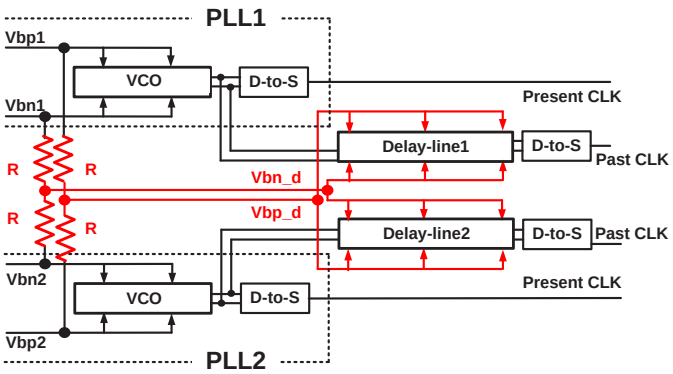


Fig. 14. Solution of the bias voltage issue using a pair of resistors.

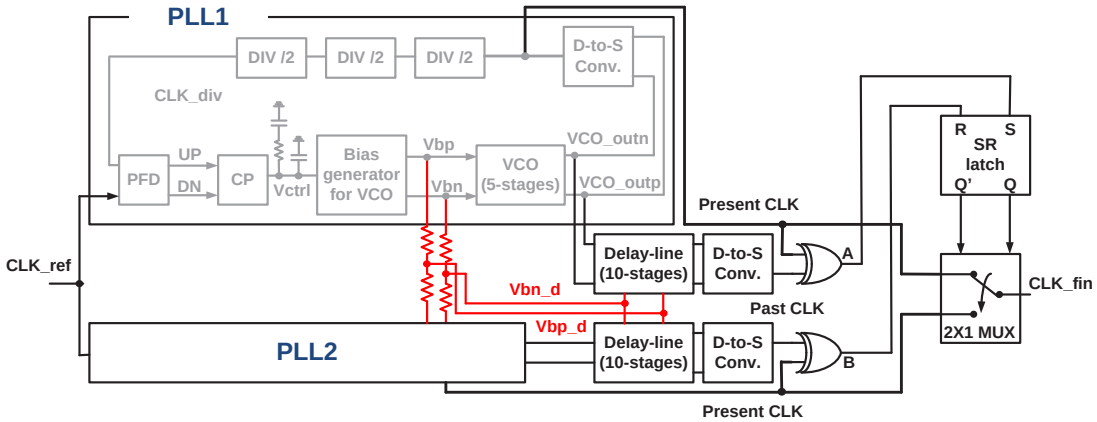


Fig. 15. Full structure of the proposed RHPLL.

3. Simulation Results

Fig. 8 shows the PLL output clock of an unhardened PLL and the final output of the proposed RHPLL after radiation-strike and their eye-diagrams. For the simulation of radiation-strike, the proposed RHPLL designed in TSMC 0.18um achieves 88.4% of cycle-to-cycle jitter improvement, which is from 1588ps to 184ps, in 2.5ns normal clock period. Compared to conventional technique' recovery time [2], this RHPLL reduce the time to recover clock periods from 35 clock cycles to 3 clock cycles. Although the recovery time depends on energy of radiation or circuit condition, the time for detection in our case is consistently 3 clock cycles.

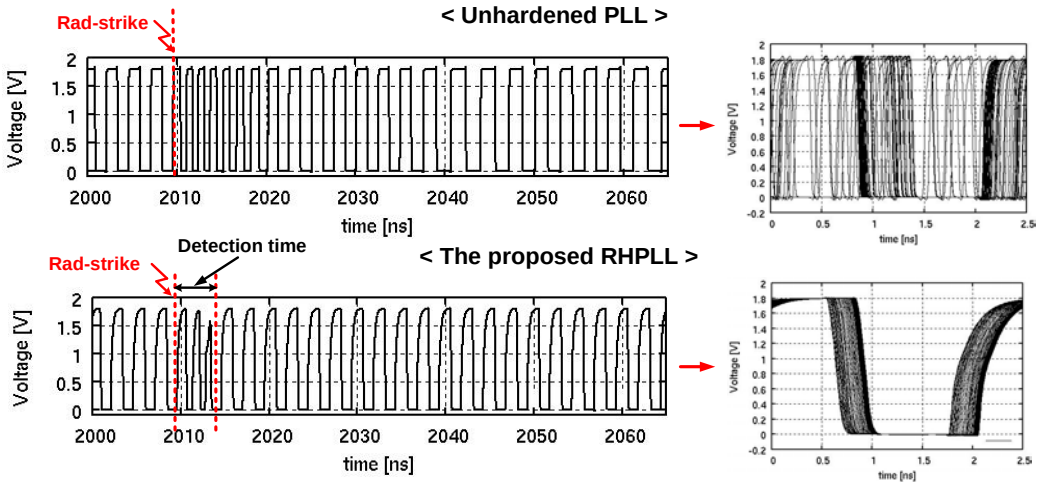


Fig. 16. Comparison of PLL output clocks and eye-diagrams between an unhardened PLL and the proposed RHPLL after radiation-strike.

4. Conclusion

A dual-PLL based on temporal redundancy for radiation-hardening is proposed in this paper. To achieve not only detection but also correction of perturbation in DMR technique, the detective circuit based on temporal redundancy is designed. This proposal has three advantages. First, it consumes less power and silicon area than the TMR technique due to use of the DMR technique. Second, all sub-circuits are protected by the DMR technique. Third, the penalties in performance are mitigated because there is no design modification of sub-circuits. As a simulation result of 400MHz PLL output clock, 1588ps of cycle-to-cycle jitter in unhardened PLL is reduced to 184ps in the proposed RHPLL.

References

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