Single Event Effects E – P2

Experimental study on radiation tolerance of SOI-PLLs

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Abstract

Single event effects on phase locked loops (PLLs) are experimentally investigated. Test chips of the PLLs are fabricated in a 0.2-μm fully-depleted silicon-on-insulator technology. The PLL architecture is designed in conjunction with hardening techniques such as the triple modular redundancy and a stacked transistor design approach. A heavy-ion beam test confirms that the hardened PLL exhibits higher radiation tolerance than non-hardened one for 7.5-MeV Ne irradiation: The accelerated ions have the linear energy transfer of 7.3 MeV・cm^2/mg in Si.

1. Introduction

Phase locked loops (PLLs) are a circuit which supplies clocks to CPUs[1]. It generates an output-clock, accelerating a slow reference clock fed to the circuit. Its radiation tolerance needs to be high enough for the right work of CPUs under radiation environments; the output-waveform of the clock is distorted when a radiation particle hits the circuit[2-5]. We have designed a PLL the radiation tolerance of which is enhanced by using a 0.2-μm fully-depleted silicon-on-insulator (FD SOI) technology in conjunction with circuit design techniques such as a triple modular redundancy (TMR) technique [6] and a stacked transistor design [7].This work reports its experimental results; see simulation results in our previous paper [8].

2.Test vehicles

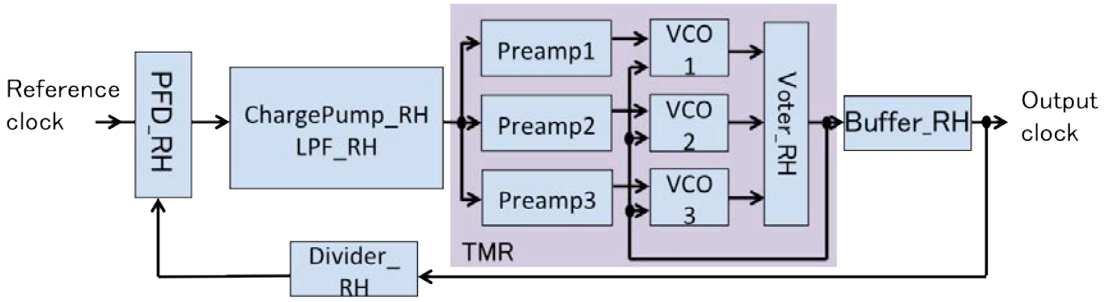

Fig.1 A block diagram of the designed SOI-PLL. PFD stands for phase frequency comparator.

Fig. 1 shows a block diagram of the tested SOI-PLL. TMR is applied to the voltage controlled oscillator (VCO) section. The stacked transistor design is applied to the all logic cells. To investigate effects of TMR, we have designed the PLL so that it can work with TMR deactivated: The power of one of the three VCO segments is kept off in this mode. In this paper, this operation mode is denoted as “non-TMR”. The other mode, where the three VCOs work harmoniously, is named “full-TMR”. The authors have fabricated test chips of the designed PLL with a radiation-hardened 0.2-μm FD SOI technology we developed [9]. To examine effects of the stacked transistor design, the chips have another “non-hardened” PLL, where neither TMR nor stacked transistor design is used.

3. Experimental tests

We have carried out a heavy-ion beam test in Takasaki Ion Accelerators for Advanced Radiation Application (TIARA) of JAEA. Ions such as 75-MeV $^{20}Ne^{4+}$ (its linear energy transfer or LET is 7.3MeV・cm^2/mg), 150-MeV $^{40}Ar^{8+}$ (15MeV・cm^2/mg), and 322-MeV $^{84}Kr^{17+}$ (40MeV・cm^2/mg) have been applied to the circuit in a vacuum chamber. The particle flux is about 5×10^3 count/cm^2/sec and the particle fluence is1×10^6count/cm^2,

which corresponds to an irradiation time of 200 sec. The circuit has been kept in operation during irradiation. The cycle length of the reference clock is fixed at 50 nsec, thus that of the output clock 10 nsec. This irradiation process has been carried out in the three various levels of mitigation technologies such as full-TMR, non-TMR, and non-hardened. During each irradiation time, to count the number of errors, we have used a trigger function of a high-speed single-shot oscilloscope(Wave Master 830Zi produced by LeCroy corporation).Errors are here defined as more than 10% changes in the cycle length of the output clock, which should be kept at 10nsec while the system works properly. Note that this measurement system is unable to detect events for 1μs after the trigger operation, i.e., the dead time is 1 μs, which is negligibly small compared to the event rates expected from the flux value. We have thus calculated the cross section according to Eq.1:

$$\text{Cross section (cm}^2) = \frac{\text{Number of errors (count)}}{\text{Flux (count/cm}^2\text{/s)} \times \text{Irradiation time (s)}}. \qquad \text{(Eq.1)}$$

These cross section measurements have been performed twice for each ion tests.

During the Ne and Kr tests, for more detailed analyses, we have recorded 50 waveforms for each irradiation time. Dynamic voltage evolution at the output is stored in each record of 5000 data points with a time resolution of 0.1nsec, thus a ±250-nsec system response is captured in total, where time "0" indicates the time at which the error is detected. From the stored waveform, to calculate the cycle lengths (T), we have read out clock edge time (t) because each cycle length is determined by the time between two adjacent clock edges. The defined clock edge time is the time when the voltage exceeds the threshold voltage (V_{th}), which is designed to be 0.25 volts. To ignore noises, ±0.05-volts margin is considered in this threshold operation (Fig. 2). Then we have drawn T - t graphs as shown in Fig.3: When a cycle length T_1 is sandwiched between two adjacent clock edges t_1 and t_2 (t_1 is earlier than t_2), we have plotted a point (t_1, T_1). This graph is representation helps us to understand cycle length modulations as a function of the elapsed time.

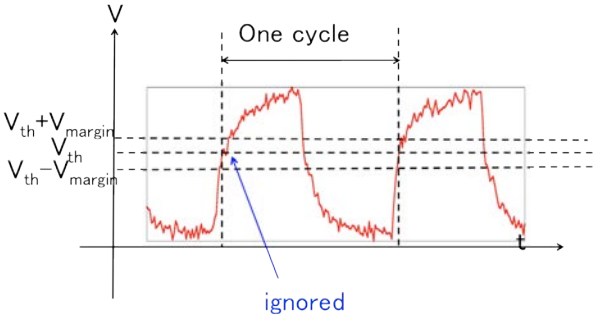

Fig .2 The define of one cycle.

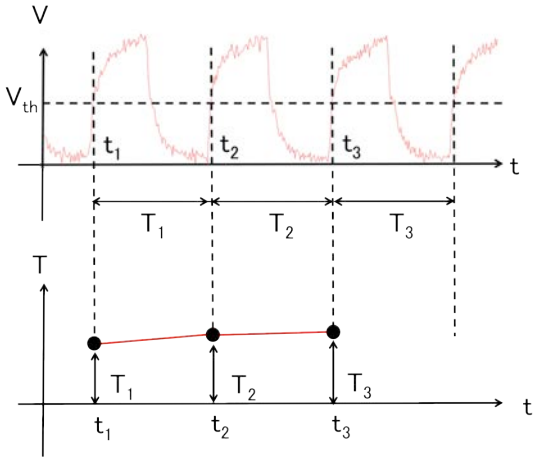

Fig.3 The way to plot the points (t,T)

4. Results

4.1cycle length modulations

Fig. 4 shows a result of cycle-length analyses. Represented by 50black lines, time-depended cycle-length modulations are extracted from 50waveforms under the Ne irradiation. The two red broken lines superimposed on the figures correspond to T = 9 nsec and 11 nsec. They represent the upper and lower boundaries of the acceptable margin. In the all circuit conditions (Fig. 4 a-c), it is observed that variations in T exceed the 10% acceptable margin at around t = 0. As the time elapses (around 100 nsec), these variations recover into the acceptable zone. These figures demonstrate that effects of a single-event transient (SET) on the PLLs continue seriously in a long time, although the original SET is as short as 100 psec [10]. The T-modulation of the non-hardened is lager and longer (Fig. 4(a)): Its max-min variance is 8.46 nsec and many of signals do not recover even after 250 nsec. Fig. 4(b) exhibits effects of the stacked transistor design (non-TMR): Its max-min variance is 5.40 nsec and most of the signals recovered at around 100 nsec. The stacked transistor design works effectively. The full-TMR exhibits the best results: Its max-min variance is 3.99 nsec and,

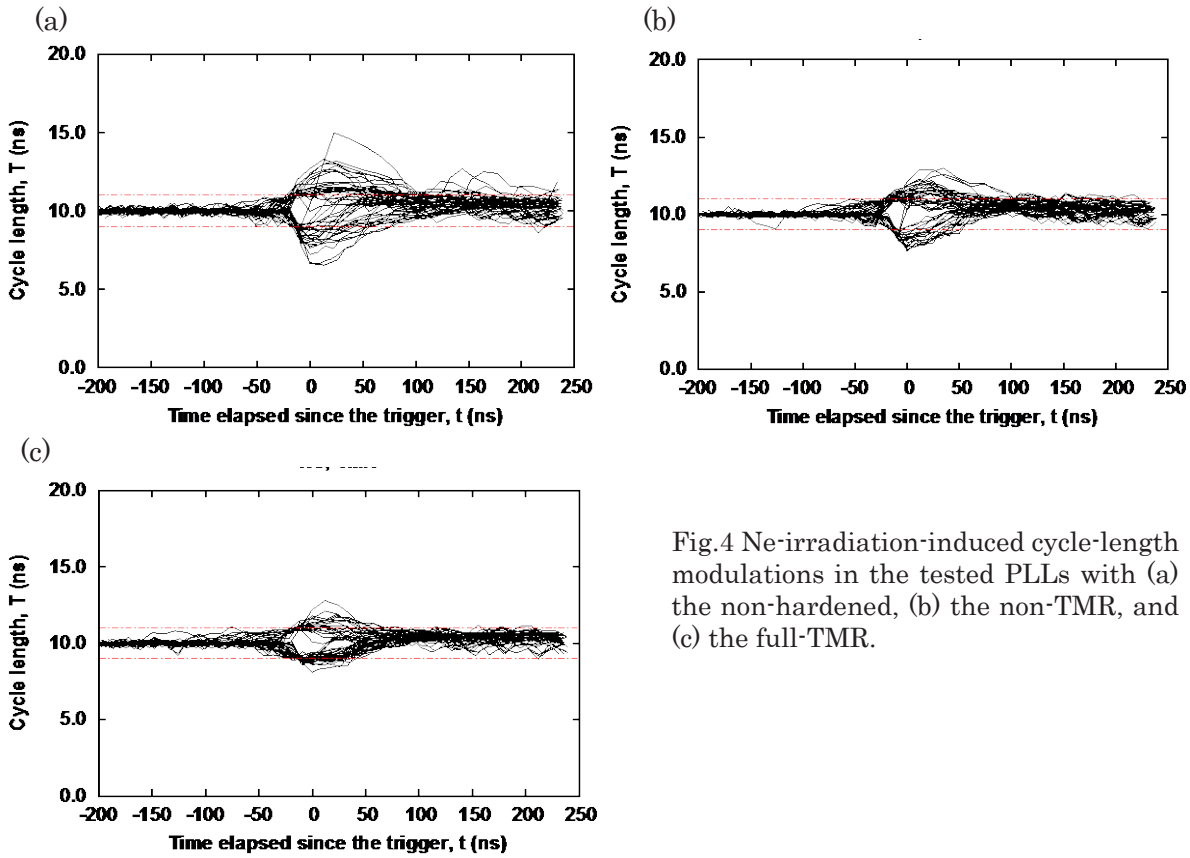

Fig.4 Ne-irradiation-induced cycle-length modulations in the tested PLLs with (a) the non-hardened, (b) the non-TMR, and (c) the full-TMR.

although a few signals are still in the error zone, almost all signals recover at around 50 nsec.

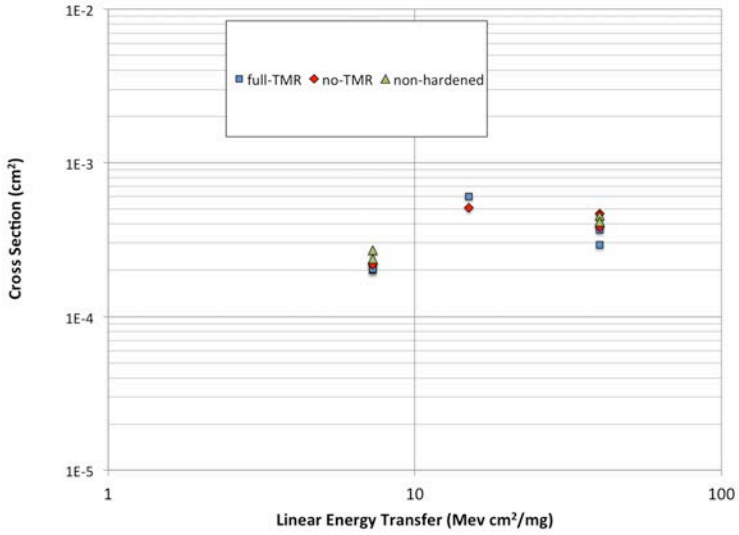

Fig. 5 The cross section-LET graph.

The TMR effectiveness is clearly observed. The Kr irradiation, on the other hand, does not exhibit this clear trend in the effectiveness of the hardening techniques, which needs further investigations.

4.2cross section

The resultant cross sections are shown in Fig.5 and summarize in Table 1. For both Ne and Kr irradiation tests, we can see the same trends as in the previous T-modulation tests.

The experimental cross sections are two orders of magnitude larger than simulation results [8]. The mitigation techniques may have some room to be improved, and there may be some circuit parts vulnerable to radiation attacks, that parts are not considered in the simulations.

Table 1 Cross sections.

Experiment	LET (MeV・cm^2/mg)	7.3(Ne)	15(Ar)	40(Kr)
	Cross section of full-TMR (cm^2)	2.0×10^{-4}	6.0×10^{-4}	3.7×10^{-4}
		2.0×10^{-4}	-	2.9×10^{-4}
	Cross section of non-TMR (cm^2)	2.2×10^{-4}	5.1×10^{-4}	4.7×10^{-4}
		2.2×10^{-4}	-	3.8×10^{-4}
	Cross section of non-hardened (cm^2)	2.7×10^{-4}	-	4.5×10^{-4}
		2.4×10^{-4}	-	4.1×10^{-4}

Simulation [8]	LET (MeV・cm^2/mg)	15	20	50	500
	Cross section of full-TMR (cm^2)	-	0.0	0.0	36.2×10^{-7}
	Cross section of non-hardened (cm^2)	3.5×10^{-7}	2.0×10^{-6}	2.1×10^{-6}	2.4×10^{-6}

5.Conclusion

We have examined radiation tolerance of PLLs that are protected by using a 0.2-μm fully-depleted SOI technology in conjunction with circuit design techniques such as a full-TMR technique for the voltage-controlled oscillator section and a stacked transistor design for the digital logic cells. The ion-irradiation results demonstrate that both techniques are effective, when LET is small, at least.

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