Consideration of Single-Event Gate Rupture Mechanism in Power MOSFET

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Abstract

The catastrophic failure mode caused by single-event gate rupture phenomenon observed in power MOSFETs still remains as a critical issue for those devices to be used in space radiation environments. Detailed analyses of the devices damaged by the phenomenon suggested a new possible mechanism. A preliminary model for the mechanism was proposed.

1. Introduction

Power MOSFETs are widely used for power handling portion of the electronic devices for space system as well as for ground-based commercial devices. However the catastrophic failure mode caused by single-event gate rupture (SEGR) in space radiation environments still remains as a critical issue for those devices.

The phenomenon of SEGR in power MOSFETs was reported for the first time in 1987 [1]. Over the past 20 years, the phenomenon was extensively characterized [2-9] and several models have been proposed to describe their mechanism [10-13]. In these studies, SEGRs are detected by abrupt increase of the gate and the drain current during heavy ion irradiation under the reverse bias condition, i.e. the device is in OFF state, according to the military specification [14]. Because the abrupt increase of the gate and the drain currents are usually observed simultaneously, it is assumed that the gate dielectric breakdown occurs between the gate and the drain. In addition to the in-situ observation, the increased gate current is measured to confirm the damage introduced by the irradiation as a post irradiation test. However, the drain terminal is tied to the source terminal for the measurement in general.

In the course of qualification test of power MOSFETs for space applications, a curious behavior was found that the leakage current introduced by SEGR phenomenon was not a simple current flowing through the damaged gate oxide area faced to the drain region on Si surface of the device die. Although the sample devices were manufactured by Fuji Electric (Tokyo, Japan) for the first observation, the same behavior was also confirmed with the devices from ST micro and IR.

To confirm the origin of the behavior, special test structures were fabricated with the manufacturing process for the p-channel power MOSFETs submitted for the qualification test. As a result of SEGR test on the test structures, it was found that the behavior was responsible to the specific structure of power MOSFETs.

In this paper, the curious behavior found in the course of the qualification test will be reviewed in detail. After the review, the results on the additional test structures will be discussed. Finally, a possible model for the mechanism of SEGRs will be proposed.

2. Review of Devices Damaged by SEGR

The irradiation test for SEGR phenomenon was carried out on the p-channel power MOSFETs for space applications manufactured by Fuji Electric. There were 2 rated voltage types, i.e. 100 and 200 V. Kr ions (768 MeV) from the cyclotron facility, RADEF, at Jyväskylä University in Finland were used for the experiments. Their LET at the device surface and range are calculated by using SRIM [15] as 32.4 MeV(mg/cm^2) and 94.1 μm, respectively. The range is sufficient to pass through the active layers of the power MOSFETs. A typical current monitor data during irradiation is shown in Fig. 1 for the device with 100 V of rated drain voltage. In this case, SEGR was observed just after V_{GS} switching from 12.5 V to 15 V. During the V_{GS} switching, the ion irradiation was interrupted. As the result of SEGR, I_{GS} and I_{DS} were abruptly increased to 2.86 mA and 690 μA, respectively. The current increases might suggest that the gate oxide was damaged and the current was injected from the gate, and flowing out to the drain and the source electrodes, because the current values were not identical. It was supposed that there were 2 current paths at least.

The electrical behavior of the damaged region introduced by SEGR has not been reported. It should be noted that the behavior cannot be explained by the model formerly proposed for SEGR mechanism [10]. According to those models, the maximum electric field is generated across the gate oxide on the drain region when an incident ion perpendicularly passes through the region. Therefore, the damaged gate oxide should be located on the drain region according to the model.

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3. Experimental

To obtain additional information on the curious behavior, the test structures were fabricated with the manufacturing process for the p-channel power MOSFETs the behavior was found. Fig. 2 shows the cross-sectional views of the test structures. The structure A has a normal power MOSFET structure for reference. For the structure B, the source diffusion was omitted. Therefore many p-n diodes are formed between the drain and the source electrodes. For the structure C, the body diffusion was formed without masking. Therefore, a large p-n diode is formed on a chip. The structure D was fabricated with the same procedure for the structure C and the source diffusion was also omitted. These test structures were fabricated on the substrates both for 100 and 200 V devices, i.e. a total of 8 types of test structures. Those test structures will be identified as 100A, 100B, and so on, in this paper.

For these structures Kr ions (713 MeV) from the RIKEN Ring Cyclotron (RRC) at RIKEN in Japan were used for the experiments. Their LET at the device surface and range are calculated by using SRIM [15] as 33 MeV(mg/cm2) and 87 μm, respectively. The range is sufficient to pass through the active layers of the test structures.

As the experimental results, SEGRs were observed for the test structures A and B. For 100 V devices, SEGRs were observed at VDS = -100V and VGS = +12.5 V. For 200 V devices, SEGRs were observed at VDS = -200V and VGS = +7.5 to +10.0 V. In contrast, no SGER was observed for the test structures C and D at VGS = +15.0V and the rated drain voltages up to a fluence of 105 p/cm2. We can conclude that

(1) SEGRs are triggered regardless of the source diffusion,

(2) the existence of the body edge is a key to trigger SEGRs.

In addition to the p-channel power MOSFETs, n-channel power MOSFETs were examined for the electrical behavior, which were already damaged by SEGR tests and stored in our laboratory. The rated drain voltages of the devices were 100 and 130 V. For those devices, Kr ions (315 MeV) from the cyclotron facility, TIARA, at Japan Atomic Energy Agency (JAEA) in Japan were used for the SEGR tests. Their LET at the device surface and range are calculated by using SRIM [15] as 40.0 MeV(mg/cm2) and 40.1 μm, respectively. The range is also sufficient for the tests. Because of n-channel devices, the polarity of the voltage and the direction of the current were opposite, but the same behavior was observed.

Additional experiments for the test structures were performed with VDS = 0V. Kr ions from TIARA were also used for the experiments. SEGRs were observed at VGS of -38 to -44 V with average of 41.6 V regardless of the structure type and rated voltage. The value is predicted by an experimentally obtained fitting equation [5] as 45.6. The values are in good agreement. However, the electrical behaviors of the damaged devices were also very interesting. For the structure A and C, only leakage current path between the gate and source electrodes was confirmed. For the structures B and D, the same I-V characteristics as structures A and B were observed.

4. Discussion

4.1 Model of the current path to the drain after SEGR

The drain current pass through the body-drain junction where no damage was observed even after SEGR might be explained by minority carrier injection effect in an analogous way for bipolar transistors. In bipolar transistors, the minority carriers are injected from the emitter to the base region, and then they can be diffused into the collector region escaping recombination in the base region even if the base-collector junction is in reverse bias condition.

In the case of power MOSFETs damaged by SEGR, the minority carriers must be injected from the gate electrode to the body region through the damaged gate oxide. Fig. 3 shows the energy band diagram to explain the hole injection observed in the damaged p-channel MOSFETs. In this diagram, it was assumed that the current path inside the oxide was formed by the localized states or damage sites and conduction occurred by hole hopping between them [16], although exact conduction mechanism had not been identified. There are several possible mechanisms for hole conduction through the damaged oxide, for example [17]. To open the hole conduction path to the valence band of the body region, the applied gate voltage need to be larger than a certain threshold level as shown inset (b) in Fig 3.

It should be noted that there are also several possible mechanisms for electron conduction through the damaged oxide [17] to explain the I-V characteristics observed in n-channel power MOSFETs damaged by SEGR.

4.2 Location of SEGR damage

As mentioned in the section II, the damage region caused by SEGR had been considered to be located inside the oxide faced on the drain region where the drain bias was applied, because the highest electric field is generated by ions perpendicularly incident in the neck region (the region between body diffusions) [10]. In contrast, the damaged region experimentally observed was located inside the oxide faced on the body region. In addition to the fact, the body diffusions must have edge in the epitaxial layer (the drain region) as islands floating in the ocean.

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According to the models for oxide breakdown [16], electrons injected into the oxide can be accelerated by the electric field applied across the oxide for impact ionization and trap creation mechanisms. This is the reason that the highest field region had been considered as the responsible region for SEGR. However the body diffusion is usually tied to the ground in normal applications of power MOSFETs. Therefore the electric field across the oxide between the gate and the body diffusion is basically separated from the electric field induced by the voltage applied to the drain and no destructively higher field is expected. However it might be possible in the power MOSFET structure to accelerate the electrons by the electric field across the body-drain junction and to inject them into the gate oxide as shown in Fig. 4. The oxide breakdown caused by hot carrier injection was studied and reported [18]. According to the study, the charge to breakdown, Q_{BD}, significantly depends on the energy of electrons injected and do not depend on the oxide field. As illustrated in Fig. 4, the electrons are generated along the ion track and accelerated by the electric field applied across the body-drain junction and injected into the gate oxide. The edge portion of the body diffusions might be more effective for the injection because of reduced thickness of the diffusions. More quantitative discussion will be made in the full paper for the mechanism.

For the cases with V_{DS} = 0V during irradiation, the electrical behaviors of the damaged devices of the structure B and D were exactly the same as the structures A and B with the rated V_{DS} was applied. The structures B and D had no source diffusion. Therefore, the electric field was applied only the gate oxide facing to the body diffusion and damage region must be introduced in the region. For the structures A and C, only the leakage current was observed between the gate and source electrode. From the behavior, it was supposed that the damaged region was located in the gate oxide facing to the source diffusion.

For n-channel power MOSFETs, hot holes can be injected into the oxide instead of hot electrons for p-channel devices. Unfortunately the hole fluence to breakdown, Qp, is not so sensitive to the energy of the injected holes according to the report [18]. There are possibilities that the drain voltage changes the injected hole fluence instead of the energy. The SEGR mechanism for n-channel device will be a future subject.
The electrical behavior observed with the power MOSFETs damaged by SEGR might be common to the devices from other manufacturers. Some of them were confirmed in our laboratory. The same behavior, i.e. I_{GS} was higher than I_{DS} at SEGR occurrence, was also found in the published paper [19].

5. Conclusion

The electrical characteristics of power MOSFETs damaged by SEGR were analyzed in detail. The analysis indicated a curious behavior and it was successfully explained by the minority carrier injection through the damaged gate oxide.
The behavior also requested a new SEGR mechanism to describe the phenomenon. The damaged spot inside the gate oxide introduced by SEGR was located on the body diffusion, where the electric field induced by incident ions had not to be so strong. The experiments with the test structures clearly indicated that the body diffusions in the epitaxial layer for the drain depletion region are responsible structure for SEGR. A possible mechanism of SEGR was proposed, where hot carriers were generated by the electric field across the body-drain junction and injected into the gate oxide. Additional work will be required to confirm the mechanism especially for n-channel MOSFETs.

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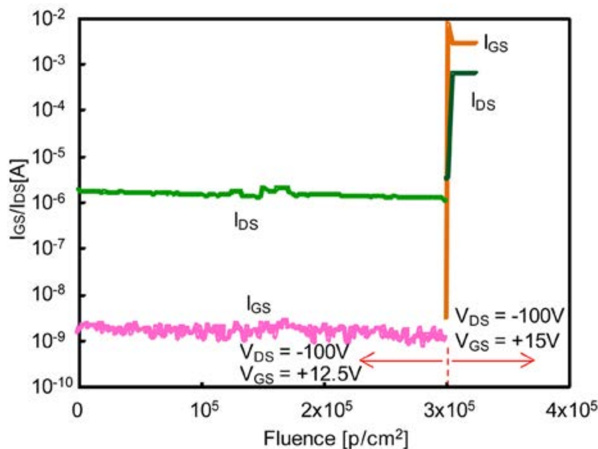

Fig. 1. Current monitor data during SEGR testing for p-channel power MOSFET with the rated drain voltage of 100 V.

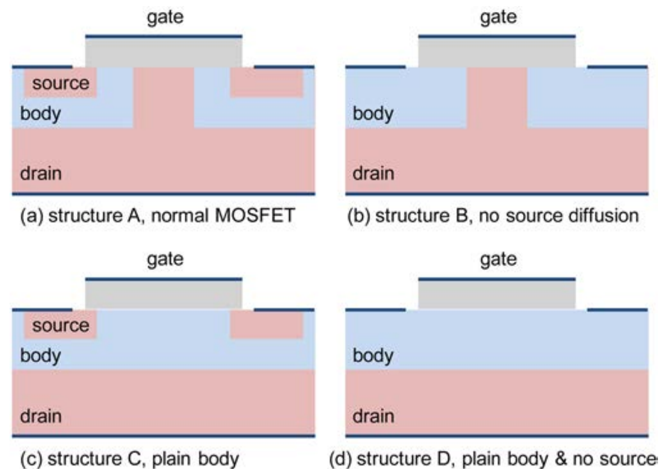

Fig. 2. Cross-sectional views of the test structures.

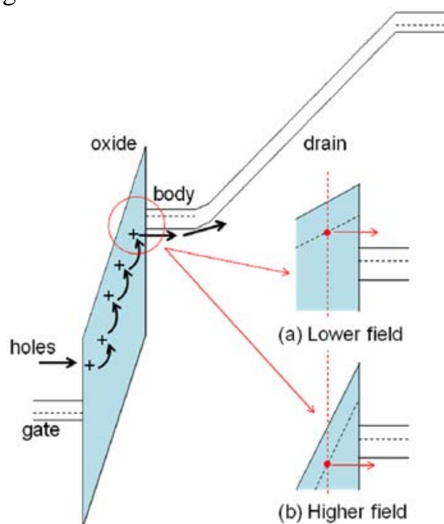

Fig. 3. Energy band diagram for p-channel power MOSFET damaged by SEGR.

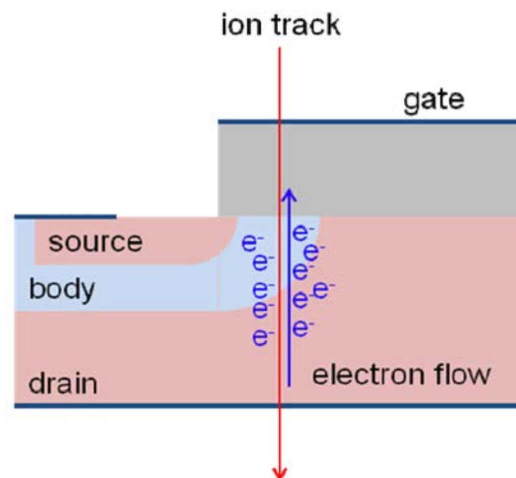

Fig. 4. Image of electron injection induced by ion strike in p-channel power MOSFETs.

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