State-of-the-Art Study on Mitigation Techniques of Single Event Effects in Terrestrial Applications

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Abstract

***Abstract*—As semiconductor device scaling is on-going far below 100nm design rule, terrestrial neutron-induced soft-error typically in CMOS devices is predicted to be worsen furthermore. Moreover, novel failure modes that may be more serious than those in memory soft-error are recently being reported. Therefore, necessity of implementing mitigation techniques is rapidly growing at the design phase, together with development of advanced detection and quantification techniques. The most advanced such techniques are reviewed and discussed.**

I. INTRODUCTION

Scaling down of semiconductor devices to sub-100nm technology encounters a wide variety of technical challenges like V_{th} variation [1], Negative Bias Temperature Instability (NBTI)[2], short-channel effect[3], gate leakage[4] and so on. Terrestrial neutron-induced single event upset (SEU) is one of such key issues that can be a major setback in scaling. As scaling proceeds below 130nm, a number of new error modes are found to be emerging. Such errors, in principle, are originated from faults or charges produced in dual or triple well regions in CMOS devices. Fault does not always cause error, depending mainly on the location and the amount of charge collected to an active node. Similarly, error does not cause always a system failure, depending on a number of masking effects in the stack layers of manufacturing processes as illustrated in Fig.1. Some failures may be fatal when they take place in the *real-time system* like avionics control system and anti-lock brake in automobiles [5]. Some other failures are not necessarily taken care of as in entertainment applications. Soft-Error Rate (SER) has been regarded as one of major metrics in reliability of electronic devices and systems, but fatality /significance of failures must be considered in designing electronic systems since we have a number of error modes in electronic systems these days.

It is generally accepted from the very beginning of terrestrial neutron soft-error issues that mitigation techniques applied to only single stack layer cannot be effective and promising solution against system failures and collaboration among stack layers has been encouraged [6,7]. In reality, such collaboration is very difficult. It may be recognized that most engineers/researcher cannot expand their specialties beyond their stack layers. Novel strategies to overcome this situation are needed to be explored and being proposed. *Built-in* communication scheme among the stack layers is proposed by Ibe, *et al.* in their LABIR (inter Layer Built-In Reliability) concept [8]. Evans *et al.* are proposing the RIIF (Reliability Information Interchange Format) as common format or protocol to be used in system design among stack layers [9].

At present, a number of SEE (Single Event Effects) prediction/detection/prevention/recovery techniques have been proposed in each hierarchy or stack layer. Such techniques are overviewed in the present paper to explore overall mitigation techniques in electronic systems against terrestrial radiation induced system failures.

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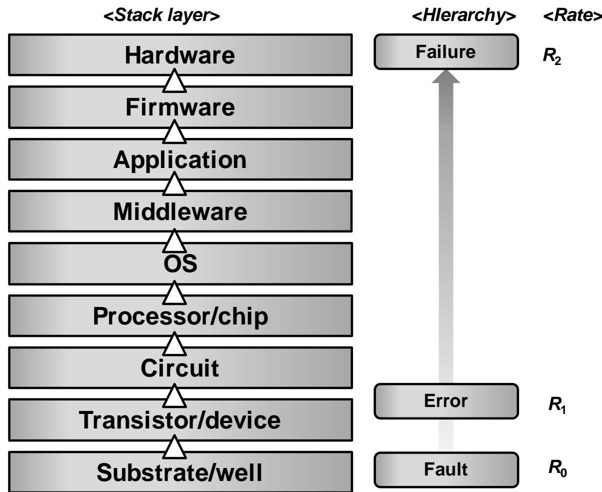

Fig. 1 Stack layers in manufacturing processes of electronic systems

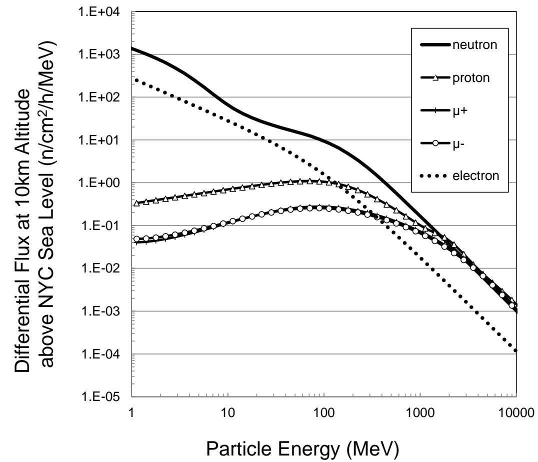

Fig. 2 Energy spectra of terrestrial radiation at NYC sea level

In addition, it is widely recognized that high-energy neutron is not unique source of terrestrial soft-error. Low energy neutron including thermal neutrons[10], protons[11], muons[12] and even electrons and photons could cause terrestrial soft-error as they are substantially present in terrestrial field as shown in Fig.2 [13]. The novel strategies must cover such global areas.

II. FALTY MODES IN EACH HIERARCHY

2.1 Fault modes

Figure 3 illustrates basic CMOS well structure. N-wells and p-wells are aligned in stripe pattern above p-substrate, and memory and logic devices are manufactured on the same well structure. As typically shown in Fig.4, charge collection mechanism take place when a charged particle pass through the storage node or bipolar action talks place when a charged particle pass through the p-n junction between the p-well and n-well. These phenomena in the well cause faults that may cause error in memory cells. The faults modes are summarized in Table 1 including stack-at fault and EMI (Electro-Magnetic Interaction).

Table 1 Fault modes and their property

Class	Definition	Name	Characteristics	In-situ detection method	In-situ recover/mitigation method
Transient/ noise	Transient in electric potential and/or current in a chip	SET[1]	Single transient due to charge collected to the diffusion layer in the chip. Pulse width is below a few nano second, and can long more than two clock pulses.	Time and/or space redundanbcy such as DMR[4], TMR[5]	None
		MNT[2]	Simultaneous SETs in more than two diffusion layers. Mainly, MNTs take place in a single well due to charge sharing or bipolar action. Space redundancy techniques such as DICE[6], TMR may not work against MNTs.	Monitoring the well potential and/or current	None
		EMI[3]	Electromagnetic noise including burst noise	Electro-magnetic probe	None
Defect	Lattice defects and or trap level in the oxides. They may cause leakage current and may disappear in time.	Vth shift	Cause of Vth shift in flash memory. They may cause stack at "0/1" error and can be permanent error.	Vth measurement	Annealing may work

1:Single Event Transient, 2:Multi-Node Transient, 3: Electro-Magnetic Interference,4: DoubleModule Redundancy, 5: Triple Module Redundancy, 6: Double Interconnect CEll

When fault take place in logic part, it is called as SET (Single Event Transient) that can cause SEU when the fault is captured in a memory element like a FF(Flip-Flop). Simple methods like parity in memory word are not effective to detect SET in logic circuit. Space redundancy

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techniques such as DMR(Double Module Redundancy) or TMR (Triple Module Redundancy) can be applied to detect SET, but they have power and area penalties. Even if MNT (Multi-Node Transient) take place in the redundant nodes, the transient cannot be detected and may cause SDC (Silent Data Corruption).

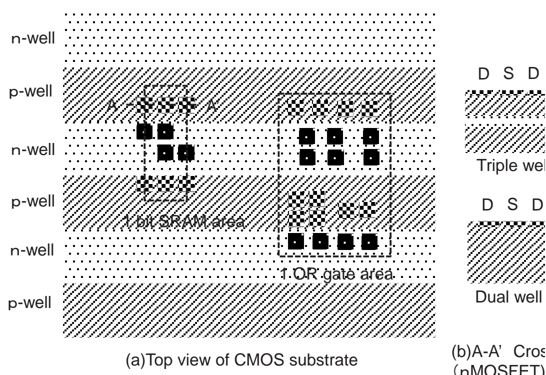

Fig. 3 Typical structure of CMOS dual/triple well and formation of a SRAM and an OR gate on the well

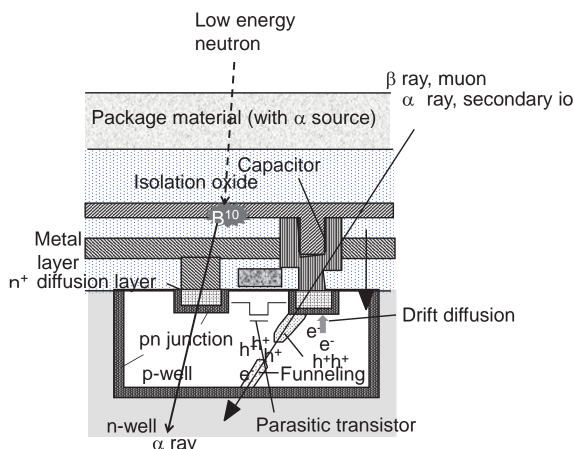

Fig. 4 Typical mechanisms of fault evolution

2.2 Error modes

Table 2 summarizes various error modes. Error modes can be classified into roughly three classes, such as soft-error or SEU(Single Event Upset), pseudo-hard error, and hard/permanent error. Soft error includes SBU(Single Bit Upset), MCU(Multi-Cell Upset), MBU (Multi-Bit Upset, MCU in the same word), MCBI (Multi-Coupled Bipolar Interaction) in memory element[14]. Direct hit on an FF by a charged particle may cause an SEU. They can be recovered by re-writing.

Table 2 Error modes of single event effects in semiconductor devices

Class	Definition	Mode name	Characteristics	In-situ Detection	In-situ recover method
SEU[1],Soft-error	Data cjhange in meomory elements such as SRAMs, Flip Flops by a single particle hit (event).	SBU[2]	Single bit error for one event.	Parity、ECC[16]	ECC
		MCU[3]	More than two bits fail in one event. Data in multiple FFs may be flipped by SET in clock line or SET/RESET lines.	Current / potential monitor	Interleave + ECC
		MBU[4]	MCU in the same word. They cannoy be corrected normal ECC.	Upper grade ECC	Upper grade ECC
		MCBI[5]	More than two bits fail locally due to potential disturbance in well by bipolar action.	Current / potential monitor	Interleave + ECC
Pseudo hard-error,PCSE[13]	Error that cannot be re-written They can mostly be activated by power cycling.	FBE[6]	Main error mode in SOI[12]. Body-tie may suppress this mode.	Parity、ECC	Power cycle
		SEL[7]	Re-writing does not work. Current continue to flow by parasitic cylyster effect. Power cycle can be applied to activate the chip.	Current / potential monitor	
		SEFI[8]	All in one definition of functional anormalities in logic circuits. Power ctcle or resetting ffs can activate the chip.SEFI in decoder in peripheral circuit of memory may cause wrong address.	FF parity/ECC	
		Firm Error	Error in configuration memory in SRAM based FPGA[14].	CRC[17]	Partial reconfiguration
Hard Error/Permanent error	Destructive and permanent error	SEGR[9]	Distruction of gate oxide in power devices mainly due to heavy ions. Flash memory can be failed by ythis mode as scaling extremely proceeds.	Anormalities in parts	Loading stand-by system
		SEB[10]	Distructive mode in power MOSFET such as IGBT[15]. SEB may take placer in IGBTs for trains and automobiles.	Anormalities in parts	Loading stand-by system

1:Sigle Event Upset, 2:Single Bit Upset, 3:Multicell upset,4:Multi-bit upset,5:Multi-Coupled Bipolar Interaction,6:Floating Body Effect, 7:Single Event Latchup, 8:Sigle Event Functional Interrupt, 9:Single Event Gate Rupture,10:Single Event Burnout, 11:Flip Flop, 12:System On Insulator, 13:Power Cycle Soft Error, 14: Field Programmable Gate Array, 15: Insulated Gate Bipolar Transistor, 16:Error Correction Code, 17: Cyric Redundancy Check

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In particular, MCUs have been under close scrutiny and their ratio to the total SEU are drastically increasing [15-19]. Though MBUs can be avoided by a combination of ECC and the interleaving technique [19], MCUs that can be corrected by EDAC/ECC can still be problematic in high performance devices such as contents addressable memories (CAMs) [20] or registers used in network processors and routers. In the case of system design, it is therefore very important to evaluate MCUs as well as soft-error rates (SERs) of the device in design phase.

Pseudo hard-error cannot be recovered by re-writing but can be recovered by resetting FFs or power cycle.
Hard/permanent error cannot be recovered by any software and may cause fatal failure. Replacement or isolation of corrupted parts is only possible method to continue to use the system.

2.3 Failure modes

Failure is defined as observable faulty condition in an electronic system, which requires actions for solution. Faults and errors can be masked sometimes without any countermeasures. To establish solution, the root cause or physical mechanisms must be identified. Classification of failures is often applied to identify the root cause or root parts/chips in a system board.[21,22]

Table 3 shows an example of such classification of failures based on the fatality of the failure with two key factors such as latency in operation and duration for recovery. When SDCs take place in a large-scale super computer, simulation may give wrong results without any latency. This type of failure is called SLFL (SiLent FaiLure). If the SDCs suffer convergence of matrix calculation or frequent rollback due to error detection, significant time loss may take place in the computer system. We call it LTFL(LaTency FaiLure). If the system requires short-range outage to recover, we can the failure LHFL (Light Halt Failure). If the system requires long-range outage, we call the failure HHFL(Heavy Halt FaiLure). It the system is un-recoverable, we call the failure FTFL (FaTal FaiLure).

Table 3 Example for classification of failure modes

Class	Definition	Mode name	Characteristics	In-situ Detection	In-situ recover method
None-latency failure	Silent data corruption in data or address that cause wrong simulation results by super computer	SLFL[1]	Soft-error takes a major role.SDC[6] causes un-recognizable mis-calculation or mis-operation.	None	（If fault level detection works） Checkpointing+ Rollback
Latency failure	Performance of the electronic system is lowered due to over frequent rollback, for example.	LTFL[2]	In case time redundancy techniques are applied, this mode is commonly take place. Typically, rollback after fault detection by using double module redundancy technique	DMR[7] error flag, the number of retries.	Reboot
Light halt dailure	Electronic system can be recovered by short-time operation.	LHFL[3]	MBU, MNT、SEL can be the cause.	ECC、current/potential monitor	Reboot/power cycling
Heavy halt failure	Electronic system can be recovered by longt-time operation. Some logs and data may be lost.	HHFL[4]	Error in the configuration memory in FPGA, SEL can cause this mode.	CRC check	Partial reconfiguration/ power cycling
Unrecoverable (Fatal) failure	Distruction of power supply and/or power device. Power supply or overall electronic system maybe exchanged.	FTFL[5]	Distruction of IGBT、DC-DC converters due to SEB.	System down	None

1: Silent Failure, 2: Latency Failure, 3: Light Halt Failure, 4: Heavy Halt Failure, 5:Fatal Failure, 6:Silent Data Corruption, 7: Double Module Redundancy

III. VISUALIZATION AND MITIGATION OF SEE

In order to establish overall mitigation techniques in electronic systems, integration of four key technologies such as prediction, detection, prevention and in-situ/off-line recovery techniques is needed. Table 4 summarizes such techniques along with two axes, stack layers and the four key technologies.

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Table 4 Visualization and mitigation techniques of SEE

Layer	Prediction/Estimation	Prevention	In-situ detection	In-situ recovery	Off-line recovery
Application	･Simulation based fault injection[r1]	･Probabilitistic calculation[r9]	･Anormally operation (e.g. SWAT[r18])	･Checkpointing-Rollback[r29]	
OS	･Log analysis		･detection mechanism in the kernel[r19]		･Reboot
PCB	･Full/partial board irradition [r2]	･DOUB (Design On Upper Bound)[r10]	･Watch-dog timer[r20]	･LABIR (inter-LAyer Built-In Reliability)[r30] ･Cross-Layer Reliability [r31]	･Reboot [r35]
Chip/Processor	･Simulation based fault injection ･Emulation based fault injection[r3] ･Irradiation test ･log analysis		･DMR (Double Module Redundancy)[r21] ･On-chip monitor [r22,r23] ･CRC[r24]	･TMR (Triple Module Redundancy)[r32] ･Chekpointing-Rollback ･Partial reconfiguration [r33]	･Reboot
Circuit	･Circuit simulation ･Logic masking simulation [r4,r5] ･Irradiation test	･Space/Time redundancy (DICE[r11], SEUT[r12], BISER[r13], SEILA[r14], LEAP[r15]) ,BCDMR[r16], RAZOR[r17]	･Parity for FFs[r25] ･BIST (Built-In Self Test) [r26]	BISR (Built-In Self Repair)[r34]	
Device	･SEE Monte-Carlo simulation [r6] ･TCAD Simulation[r7] ･Irradiation test	･Addition of resistor and/or capacitor ･Confinement of charge collection vollume ･Gate sizing	･ECC, parity	･ECC (SBU only) ･Data mirroing	
Substrate/well	･TCAD Simulation[r8]	･Enhancement of migration ･Optimization of well structure/size	･BICS (Built－In Current Sensor) [r27,r28] ･BIPS (Built-In Pulse Sensor)		

[r1] A. Evans, et al.(2012)
[r2] K. Shimbo, et al.(2011)
[r3] P. Roche(2010)
[r4] T. Takata, et al.(2010)
[r5] T. Talkata, et al.(2011)
[r6] E. Ibe, et al. (2001)
[r7] H. Yamaguchi, et al.()
[r8] E. Ibe, et al(2006)
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[r31] J. Loncaric(2011)
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[r33] M. Abdelfattah (2012)
[r34] K.Z. Pekmestzi, et al.(2008)
[r35] K. Shimbo, et al.(2011)

The explanations on the following columns in Table 4 are skipped here because of space limitation.

3.1 Prediction/estimation techniques
3.2 Prevention Techniques
3.3 In-situ detection
3.4 In-situ recovery

3.5 DOUB (Design On Upper Bound) and LABIR (inter- LAyer Bulit-In Reliability)

In the Sections 3.2 and 3.4, stack layer (device, circuit, module/processor) level prevention/recovery techniques are reviewed and no single mitigation technique seems to fulfill simultaneously the reliability and performance requirements with minimum penalties and reasonable costs.

The authors, therefore, are working on the different and novel approach named (v) Design on Upper Bound (DOUB) by which the upper-bound failure rate can be estimated explicitly.

The equation (A), for example, gives the maximum upper-bound of chip-level SET because the equation does not include any masking effects. By modifying the maximum upper-bound with various physical limits determined by device structure/layout, circuit complexity, structure of logical layers, the realistic upper-bound failure rate free from the variations may be obtained. Figure 7 shows an example of such cumulative upper bounds of fault rates for various radiation sources calculated from the spectra in Fig. 2. If this upper-bound of a chip is low enough, the chip can be ignored for further analysis. If the upper-bound is of concern, mitigation techniques are applied from a simple and low cost method in design phase as shown in like:

By using soft-error Monte-Carlo simulator CORIMS, the author also tried to calculate upper-bound fault rates for various terrestrial radiation, and obtain some important conclusions:

(i) Exchange of weak logic gate/memory to robust logic gate/memory. DRAM is currently very robust device and can be substitute of SRAMSs where speed is not critical [33,34].

(ii) Minimization of active memory area

(iii) Limited and local use of space or time redundancy techniques in the circuit level, and so on.

The authors are proposing a novel method LABIR (Inter LAyer Built-In Reliability) as is illustrated in **Fig.8**. LABIR proposes interactive or communicative mitigation techniques in which a recovery action such as rollback to the checkpoint ignited when a layer finds any error symptom, not necessarily error or fault itself. BIST (Built –In Self Test) [47], Built-In Current (Pulse) Sensor (BICS[48], BIPS) can be used for such kind of technique for symptom detection. The symptom may

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not appear so often so that power and area penalties can be minimized with minimum additional structure and circuits. By using BIPS, a pulse current propagated from an MCBI (Multi-Coupled Bipolar Interaction) zone in p-well can be detected in I_{dd} line as demonstrated in [14]. By capturing such a symptom by applying a sense amp between adjacent two p-wells, for example, errors or failures can be resumed by the rollback and replication operation in CPU level of the ULSI chip. Other sources of noises like EMI (Electro-Magnetic Interference) [35] propagate in wider area than soft-error over many wells so that they can be eliminated by the differential method between adjacent wells.

CONCLUSIONS

As semiconductor device scaling is on-going far below100nm design rule, terrestrial neutron-induced soft-error typically in SRAMs is predicted to be worsen furthermore.

Moreover, novel failure modes that may be more serious than those in memory soft-error are recently being reported. Therefore, necessity of implementing mitigation techniques with marginal penalties including power dissipation is rapidly growing at the design phase, together with development of advanced detection and quantification techniques. The most advanced such techniques are reviewed and discussed with proposal of novel mitigation strategies of the Design on Upper Bound (DOUB) and the inter LAyer Bulit-In Reliability (LABIR).

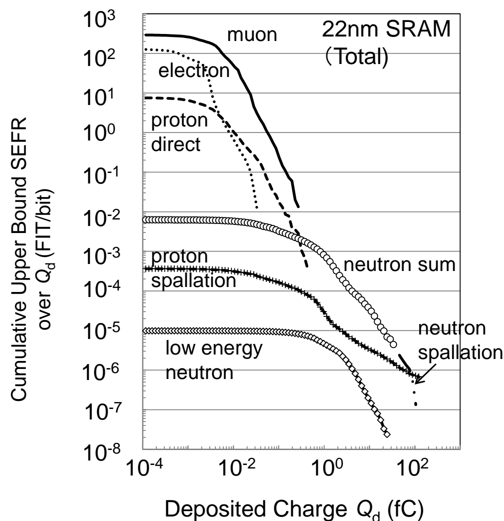

Fig. 7 Cumulative upper-bound fault rates due to various radiation sources at NYC sea level calculated by using CORIMS

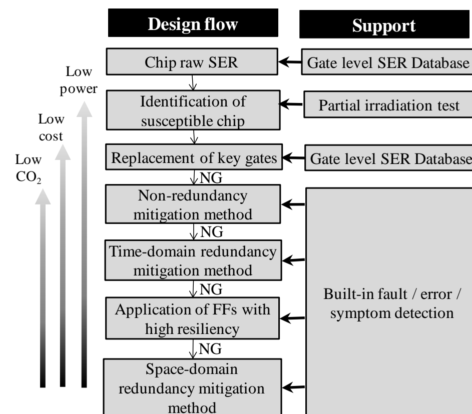

Fig. 8 General design flow of stepwise reduction in SER under the design on upper bound concept. Power consumption, cost, and global warming are key issues.

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