Measurement of Distance-dependent Multiple Upsets of Flip-Flops in 65nm CMOS Process

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Abstract

We measured neutron-induced SEUs (Single Event Upsets) and MCUs (Multiple Cell Upsets) on FFs in a 65 nm bulk CMOS process. Measurement results show that maximum MCU / SEU ratio is 30.6% and is exponentially decreased by the distance between latches on FFs.

1. Introduction

As process scaling, MCU is becoming one of the most significant issues for LSI reliability since it cannot be removed by ECC [1], [2]. In a 65 nm process, MCUs are observed in FFs and increase soft-error rates of radiation-hardened FFs [3]. Since MCU rates depend on the cell-distance, redundant latches on radiation-hardened FFs are separated over 1.1μm for high error resilience in [4]. To increase soft-error resilience, it is necessary to measure characteristics of MCUs on FFs.

In this paper, we show measurement results of neutron-induced SEUs and MCUs on D-FFs in a 65 nm bulk CMOS process to evaluate the dependences of the distance of FFs.

2. Test Chip Structure

To measure neutron-induced MCU and SEU on FFs, three different shift registers are implemented as shown in Fig. 1. They have 0μm, 1μm, or 2μm horizontal displacements between odd rows and even rows. They are implemented in order to measure MCU rates by changing the distance between master latches or slave latches on FFs as shown in Fig. 2. They have tap-cells (well-contacts) which are inserted every 50 μm.

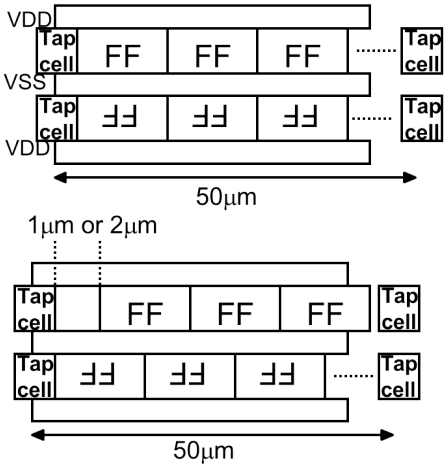

Fig. 1 Layout structures of shift registers.

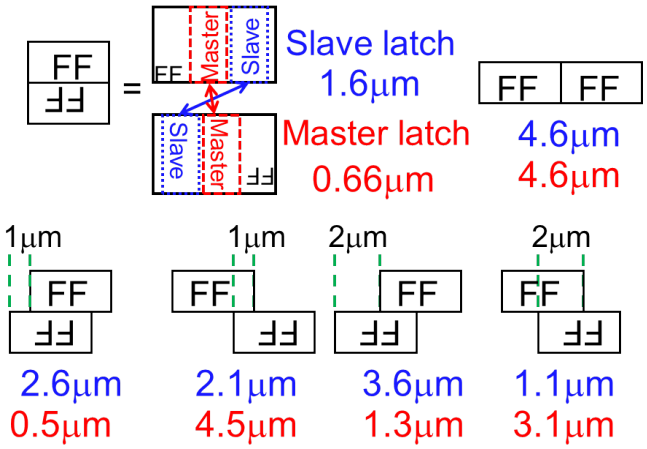

Fig. 2 Distance between master or salve latches on FFs.

3. Experimental Setup

Fig. 3 shows a chip micrograph fabricated in a 65 nm bulk CMOS process on a twin-well structure. Each shift register includes 10k FFs. The total area of four shift registers is 0.5 x 0.6 mm^2 on a 2 x 4 mm^2 die. Accelerated tests were carried out by spallation neutron irradiation at RCNP (Research Center for Nuclear Physics, Osaka University). The average acceleration factor is 3.8 x 10^8 compared with ground level of Tokyo. To increase soft error counts, 28 chips are measured simultaneously by using stacked DUT boards as shown in Fig. 4. During irradiation, clock signal is fixed to “1” or “0” to keep master or slave latches on FFs in the hold state. All stored values of the FFs were retrieved every 5 minutes.

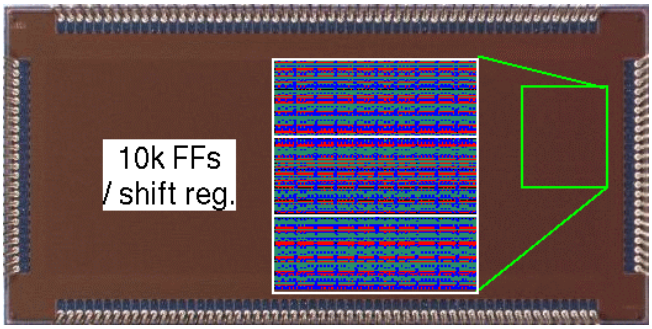

Fig. 3 Chip micrograph with floorplan.

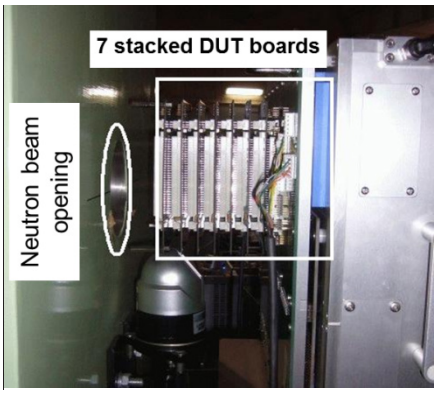

Fig. 4 Stacked DUT boards

4. Experimental Results

Table I shows the number of SEUs and MCUs of the shift registers as shown in Fig. 1. The maximum MCU / SEU ratio is 30.6% which is close to that on 65 nm SRAM cells [5]. These results clearly show that soft-error resilience of redundant FFs flipped by MCUs is only 4 times higher than non-redundant FFs and MCU mitigation design is necessary for redundant FF to improve soft error resilience. We observe more than 3-bit MCUs as shown in Fig. 5. We assume that 5 to 8-bit MCUs are caused by successive hits [6] since they spread in line.

Fig. 6 shows the distance-dependence of MCU / SEU ratios on FFs. MCU / SEU ratios are exponentially decreased according to $d^{1.68}$ (d is the distance between two latches) and fitting line shows that they can be 100% when $d \leq 30$ nm. To achieve 100x higher soft-error resilience in redundant FFs than in non-redundant FF, we must implement redundant FFs whose latches are separated by 4 μm from each other. However, it consumes huge area or complicated design procedures and these drawbacks cannot be reduced by the process scaling.

Table 1 The Number of SEUs and MCUs by neutron irradiation

	# of SEU	# of MCU	MCU/SEU ratio[%]
FF	507	110	21.6
FF with 1μm displacement	487	148	30.6
FF with 2μm displacement	567	91	16.2

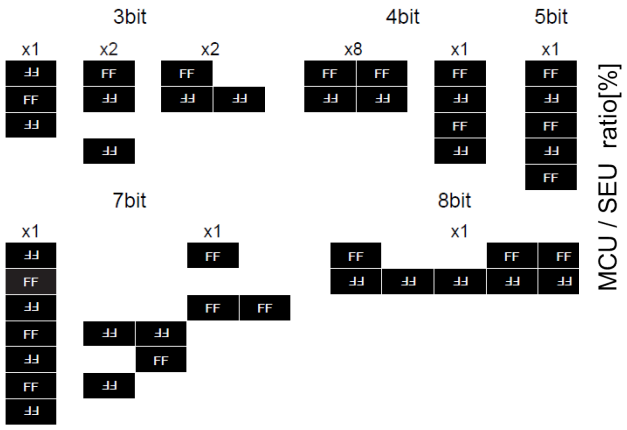

Fig. 5 MCU patterns with more than 3 FFs flipped

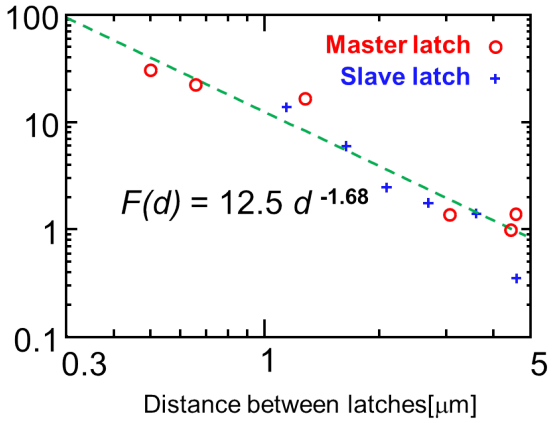

Fig. 6 Distance-dependence of MCU

5. Conclusion

We measured neutron-induced MCUs on FFs in a 65 nm CMOS process in order to evaluate their dependences on the distance of FFs. Accelerated test results show that the maximum MCU / SEU ratio is 30.6% and is exponentially decreased by the distance of latches. To achieve 100x higher soft-error resilience in redundant FFs than in non-redundant FF, we must implement redundant FFs whose latches are separated by 4 μm from each other.

Acknowledgments

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