Built-In Self-Test Circuit for Total Ionizing Dose Radiation Effects in Analog-to-Digital Converters

Esko O. Mikkola*[1], Viraj S. Pandit[2], Byoung Uk Kim[1], and Andrew Levy[1]

[1] Ridgetop Group, Inc., USA
[2] Novellus Systems, Inc., USA
*Email: Esko.Mikkola@RidgetopGroup.com

Keywords: Built-in self-test (BIST), Total ionizing dose (TID), Radiation Effects, Analog-to-Digital Converter (ADC)

Abstract

Innovative Built-In Self-Test (BIST) circuit for monitoring Total Ionizing Dose (TID) radiation effects in Analog-to-Digital Converters (ADC) is presented.

Introduction

Total ionizing dose (TID) effects remain a significant problem in analog-to-digital converter (ADC) design, despite the trend of improving TID hardness of deep submicron CMOS technologies. High-resolution ADCs require high-gain analog components, such as operational transconductance amplifiers (OTA). The high open loop voltage gain in these amplifiers is normally achieved by stacking several transistors on top of each other in cascodes, which requires the use of analog power supply voltages higher than the thin gate oxides of standard deep submicron nanotechnology CMOS transistors can withstand. Moreover, it is preferable to use higher power supply voltages in order to maximize the converter signal-to-noise ratio (SNR) in the presence of thermal noise. Hence, older CMOS technologies or thick-oxide I/O transistors available in newer technologies are still commonly used for ADC designs, thus TID remains a problem.

One of the main challenges has been the TID-induced offset errors in analog and mixed-signal circuits, such as amplifiers and comparators. These offset errors can be caused by TID-induced threshold voltage (V_T) shifts and/or leakage currents [1]. Systems containing these building blocks, such as ADCs, have been shown to be particularly “soft” for TID in numerous studies and tests. Several types of failures, such as missing codes [1], [2], increased non-linearity [1-6], increased power supply current [3-5], degraded internal reference voltage [4-6], and increased gain error [7] have been shown to occur in ADCs after only 5 to 60 krads of TID.

This paper describes an innovative BIST system that can be used to monitor TID-induced performance degradation effects in ADCs, such as increased differential non-linearity (DNL), integral non-linearity (INL), gain error, offset error, and missing codes. The BIST system is designed in a commercial 0.25 μm CMOS process. The digital and mixed-signal circuit blocks have been simulated and verified through VHDL, VHDL-AMS, and SPICE simulations in the Dolphin SMASH® simulation environment. Radiation effect simulations were performed in VHDL-AMS to prove the effectiveness of the BIST circuit in capturing the TID-induced parameter drifts in a commercial 8-bit ADC.

Total Ionizing Dose Radiation Effects

The TID damage pertains to a cumulative charge collection and trapping in semiconductor oxides caused by ionizing radiation over the exposition time. It is measured in rads, and can cause slow gradual degradation in IC performance. Trapped charge in the gate oxide of an NMOS device causes a V_T shift, which further can cause an offset in an analog circuit that the transistor is used in. The TID-induced V_T shift does not seem to be a concern for CMOS generations of 180 nm and smaller [9]. It is assumed that this increase in TID hardness is caused by the reduction of the gate oxide thickness below the intrinsic tunneling length of SiO_2.

The other TID effect type is the leakage current that is caused by inversion of the silicon adjacent to insulation trench oxides that contain trapped charge. The severity of this effect has been significantly reduced in modern nano-CMOS fabrication processes. This is thought to be caused by several factors, one of which is the increased STI sidewall doping in the modern processes [10]. The TID-induced leakage current is still a concern for CMOS fabrication processes commonly used to design analog and mixed-signal circuits (0.18 to 1.0 μm), such as ADCs, and for I/O transistors of modern deca-nanometer processes [10].[1] The severity of the TID problem in ADC circuits can be seen in studies where top-of-the-line commercial ADCs were shown to manifest parameter drifts

[1] The TSMC 0.25 μm CMOS process, used for the designs in this paper, has been shown to have a severe leakage problem and a minor V_T shift problem in radiation environments that are comparable to the environment of the Earth orbiting satellites [9].

that render them useless after only 5 to 60 krads of TID [2-7]. It is obvious that there is a need for BIST circuits that can monitor changes in most critical ADC parameters in radiation environments.

BIST Design Overview

We have designed a BIST system that can be used to accurately self-test TID effects in different types of ADCs. The ADC performance metrics that can be tested with this BIST system are missing codes, offset error, gain error, differential non-linearity (DNL) and integral non-linearity (INL). A block diagram of the developed BIST system is shown in Fig. 1. This particular BIST design is optimized for monitoring TID effects in ADCs with resolutions up to 10 bits. Our test ADC is a commercially available 8-bit, 20 megasamples per second (MS/s), sub-ranging two-step converter [11]. For testing higher ADC resolutions, the basic circuit topology remains the same but the resolution of the delta-sigma digital-to-analog converter (DAC) in the system needs to be increased. For accurate BIST operation, the DAC resolution should be 2 to 4 bits higher than the resolution of the tested ADC. Since the conversion speed of the DAC is not critical in this BIST design, the resolution of the delta-sigma DAC can be increased by increasing the oversampling ratio (OSR). DAC resolutions up to 18 bits can be achieved, which allows self-testing of ADCs with up to 16 bits of resolution with this technique.

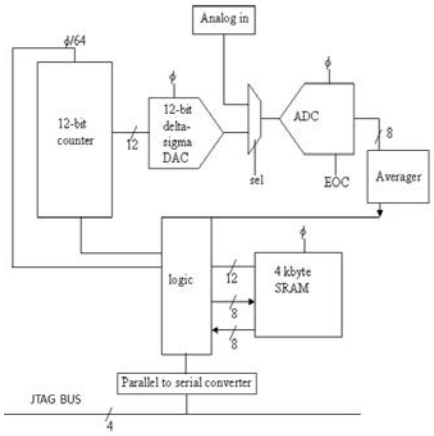

Fig. 1. The BIST system block diagram.

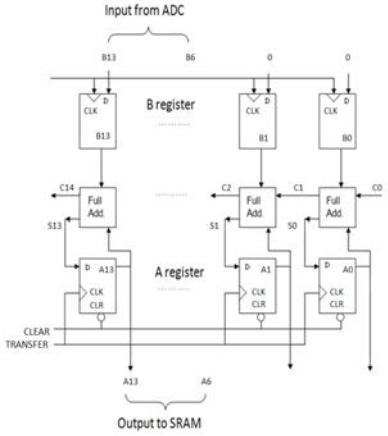

Fig. 2. Averager block diagram.

The operation of the BIST circuit in Fig. 1 is discussed next. A 12-bit counter creates the digital code input for a 12-bit delta-sigma DAC that outputs a highly linear analog voltage ramp that is used as the test bias of the 8-bit ADC. An analog multiplexer (MUX) at the input terminal of the ADC selects between the normal ADC input (shown as “Analog in” in Fig. 1) and a test bias used during a BIST cycle. A BIST cycle can be executed any time during normal operation. During a BIST cycle, the ADC samples the test signal at its nominal sampling rate, which in this case is 16 MS/s. Since the tested ADC is much faster than the high-OSR DAC, a large number of digital data for every voltage step in the input ramp will be created. These data may be stored in an off-chip memory.

Our application requires an area-intensive on-chip radiation-hardened memory, thus a special data averaging subcircuit was created to reduce the amount of data that needed to be stored. This subcircuit is called Averager in Fig. 1. The Averager computes the arithmetic average of 64 consequent ADC conversion results, and stores this average into an on-chip 4 kilobyte radiation-hardened SRAM memory. The Averager consists of digital full adders and shift registers. Its block diagram is shown in Fig. 2. Without this subcomponent, a much larger 320 kbyte on-chip memory would be needed. The control interface to the BIST circuit is a JTAG bus, which requires a serial data stream from the BIST. Thus, a component that converts the SRAM 8-bit parallel output into serial form is needed. An 8-bit parallel-to-serial converter was designed for this purpose. The last designed subcircuit is a control logic block that communicates between different subcircuits in the BIST system.

Due to area constraints, the BIST system does not contain on-chip logic that directly calculates TID-induced ADC parameter changes, such as changes in DNL and INL. The data stored in the SRAM can be accessed via the JTAG connection and the TID effect characterization will be performed off-chip. The format of the data stored in the memory is optimized for a characterization technique called “ramp histogram method” that can be used for missing code, gain error, offset error, DNL and INL characterization [2], [12]. All the parts in the BIST system have to be hardened against TID and tolerant to single-event effects (SEE). This can be done by using standard radiation-hardened-by-design (RHBD) techniques, such as the enclosed gate layout technique, guard rings, DICE cells, and triple modular redundancy. The fact that the operation frequency of the BIST circuit is

slow makes the implementation of these techniques easier.[2]

Tested ADC

The 8-bit, sub-ranging, two-step ADC used as the test device is designed [11] and manufactured by Ridgetop Group, Inc. located in Tucson, Arizona. The SPICE net list for the circuit, provided by Ridgetop, was used as a basis for the VHDL-AMS model design in this project. The 8-bit ADC consists of two flash-type 4-bit sub-ADCs. The voltage range between positive and negative reference voltages (REF+, REF-) is divided into several "internal" reference voltage values with a resistor ladder. These node voltages are connected to the reference voltage nodes of an array of comparators. The comparator array compares the input signal voltage to these reference values and outputs digital thermometer code. The thermometer code is then converted to the ADC digital output with decoder logic. An N-bit full-flash ADC has 2^N-1 comparators. Thus, a 4-bit flash has 15 comparators.

Ridgetop's 8-bit sub-ranging, two-step ADC consists of two of the above-described 4-bit flash-ADC components and control logic. The first 4-bit sub-ADC is used for extracting the four most significant bits (MSB) and the second sub-ADC extracts the remaining four least significant bits (LSB). The resistor ladder consists of 16 "large" resistors, each of which is actually formed by 16 "small" resistors connected in series. The 16 "large" resistors provide the reference voltages for the MSB converter. The MSB converter provides the four MSB bits and also controls the sub-ranging process for the LSB converter. The LSB comparator array connects to a "small-resistor" sub-range when the MSB conversion is done, and then performs the LSB conversion. The location of the sub-range, which the LSB converter connects to, is based on the MSB conversion output. The MSB and LSB bits are stored in the output registers.

Radiation Effect Simulation

The effectiveness of the BIST circuit in monitoring TID effects in ADCs was demonstrated by HDL simulations. The TID effects in the ADC circuit were modeled with a VHDL-AMS-based method that has been previously developed and published by the authors [1], [14]. In this method, TID-induced leakage currents are modeled with parasitic transistor models in SPICE simulations for basic circuit blocks, such as voltage comparators. Then these simulation results are used to construct accurate behavioral simulation models for larger circuits and systems, such as ADCs.

A VHDL-AMS simulation result for the 8-bit ADC which includes 500 krad TID models is shown in Fig. 3. The VHDL-AMS simulator was SMASH® by Dolphin Integration [15]. When this figure was created, the output of the ADC was converted back to analog format with an ideal DAC to make the radiation effect observations easier for the reader. The input to the ADC in this transient simulation is the high-linearity slowly increasing analog voltage ramp created with the 12-bit DAC in the BIST system. It's clearly seen that the radiation-induced offsets in the 8-bit ADC circuit cause severe distortions (missing codes) in the output. These missing codes are caused by voltage offsets generated in the comparators of the MSB flash ADC. These offsets cause the LSB comparator to get momentarily connected to a wrong sub-range, causing a 4-bit decrease in the resolution of the full converter, which can be clearly seen in the ADC output curve in Fig. 3.

To prove the functionality of the BIST circuit, the data stored in the 4-k SRAM block after a simulated self-test cycle are plotted (shown in Fig. 4; note that the digital code is converted to analog format with an ideal DAC again to make the radiation effect observations easier for the reader) and compared to the data directly measured at the ADC output (Fig. 3). As can be seen, the two curves are (almost) identical. After more in-depth evaluation, it was found that the data stored in the memory during the BIST cycle are an accurate representation of the distorted signal directly measured at the ADC output. This proves the functionality and effectiveness of the BIST design.

[2] The authors have previously published an innovative technique that can be used to harden the comparator in the delta-sigma DAC against single-event transients [13].

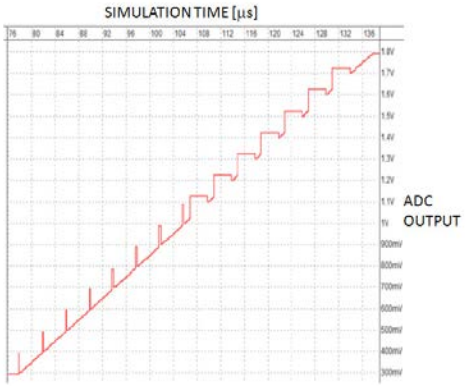

Fig. 3. Simulation with TID models show that the ADC output is severely distorted by missing codes after 500 krads of TID stress.

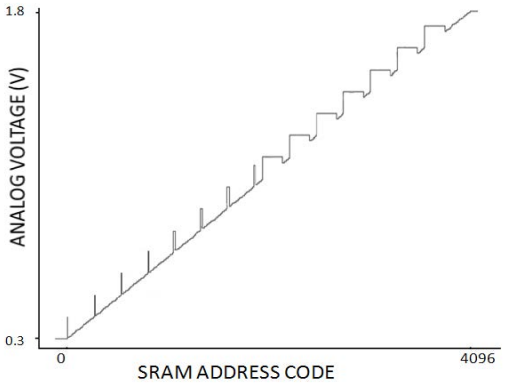

Fig. 4. The codes stored in the SRAM during the BIST cycle show exactly the same distortion effects as observed in the output of the ADC, proving the functionality of the BIST system.

Summary

An innovative built-in self-test (BIST) circuit for TID effects in analog-to-digital converters is presented in this paper. The BIST circuit can be used to monitor TID-induced performance degradation effects in ADCs, such as missing codes, increased DNL and INL, and increased gain error and offset error. Functionality of the designed BIST circuits and the effectiveness of the system in monitoring TID effects in a commercial ADC were verified through rigorous electrical and radiation effect simulations in SPICE and VHDL-AMS.

Acknowledgments

The authors wish to thank Sara Nation from NAVSEA/Crane and Ridgetop Group, Inc. for sponsorship of this work. In addition, the authors wish to thank A. Vaddigiri, E. Grubbs and U. Padmanabhan from the Electrical and Computer Engineering Department at The University of Arizona, Tucson, AZ, USA; B. Vermeire from Arizona State University, Tempe, AZ, USA; and Lucile Rey de Nardo from Dolphin Integration, Meylan, France.

References

E.O. Mikkola, B. Vermeire, H.G. Parks, R. Graves, “VHDL-AMS modeling of total ionizing dose radiation effects on CMOS mixed signal circuits,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 4, part 2, pp. 929 – 934, Aug. 2007.

Sharma, A.K., et al., “Evaluation of high performance converters under low dose rate total ionizing dose (TID) testing for NASA programs,” Radiation Effects Data Workshop, IEEE 1998, Page(s): 142 – 147.

Black, J.D., et al., “Total dose evaluation of state-of-the-art commercial analog to digital converters for space-based imaging applications,” Radiation Effects Data Workshop, IEEE 1998, Page(s): 121 – 126.

C.I. Lee and A.H. Johnston , “Comparison of total dose responses on high resolution analog-to-digital converter technologies,” *IEEE Trans. Nucl. Sci.*, vol. 45, no. 3**,** Jun. 1998.

Tomasch, G., et al., “Co-60 total dose test of 14- and 16-bit ADCs,”Radiation Effects Data Workshop, 2000, Page(s): 26 – 31.

Layton, P., et al., TID performance degradation of high precision, 16-bit analog-to-digital converters Radiation Effects Data Workshop, 20, IEEE , Page(s): 6 – 10.

H. Nakajima, et al., “Performance of an Analog ASIC Developed for X-ray CCD Camera Readout System Onboard Astronomical Satellite, “ IEEE Transactions on Nuclear Science, Vol. 56, No. 3, June 2009.

M. Shadfar, Z. Navabi, “BIST modeling and its application in design verification”, eda.org VIUF Proc, pp. 4.17-4.21, 1995.

R.C. Lacoe, “Improving integrated circuit performance through the application of hardness-by-design methodology,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, Aug. 2008.

M. McLain, H.J. Barnaby, K.E. Holbert, R.D. Schrimpf, H. Shah, A. Amort, M. Baze, and J. Wert, ‘‘Enhanced TID susceptibility in sub-100 nm bulk CMOS I/O transistors and circuits,’’ *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, Dec. 2007.

InstaCell ADC-8-100 Analog to Digital Data Converter IP Data Manual, Ridgetop Group Inc., Tucson, AZ: 2005. Available: http://www.ridgetopgroup.com

S. Cherubal, A. Chatterjee, “Optimal INL/DNL testing of A/D converters using linear model”, *ITC Int. Test Conf..*, IEEE 2000.

E.O. Mikkola, B. Vermeire, H.J. Barnaby, H.G. Parks, and K. Borhani, “SET tolerant CMOS comparator,” *IEEE Trans. Nucl. Sci.*, Dec. 2004.

E.O. Mikkola, B. Vermeire, T. Chiu, H.J. Barnaby, H.G. Parks, “Total dose radiation effect simulations on a high-precision data acquisition system”, *IEEE Trans. Nucl. Sci.*, RADECS 2007 Special Issue, Aug. 2008. (Submitted for publication)

SMASH Mixed-Signal Simulator, http://www.dolphin.fr/medal/smash/smash_overview.php