PLASMA ESD QUALIFICATION TEST PROCEDURE OF ALCATEL SPACE SOLAR ARRAY

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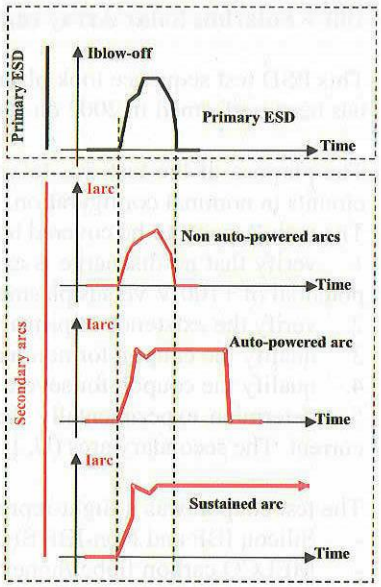
Abstract

The detrimental effects of spacecraft charging are well known, particularly when the charging leads to arcing on solar array and consequently to permanent power loss. Motivated by these concerns, ALCATEL SPACE has undertaken several test campaigns to qualify solar array design and to investigate margins.
This paper describes the state-of-the-art of ALCATEL SPACE solar array ESD laboratory test set-up and procedure. The primary discharges are created using a plasma source and a negative polarisation of the sample rear side. The required power to feed the arc can be delivered by a Solar Array Simulator with low capacitance power sources. The test sample is fully representative of a flight model.

Introduction

Based on several solar array ESD test campaigns and a fruitful collaboration with ONERA-DESP & CNES experts, ALCATEL SPACE has defined a solar array ESD qualification test procedure using a plasma or ion source. This solar array ESD qualification test procedure is considered to be conservative and valid for panels using Silicon solar cells. The breakdown limits identified by these test results are consistent with the detected failures in orbit.
The ALCATEL SPACE Silicon solar array geostationary flight heritage, qualified with this ESD test procedure, is very large **and corresponds to 30 cumulated years** in orbit. This heritage includes the new solar array family : SOLARBUS (5 solar arrays currently in orbit). The SOLARBUS family range is based on a standard panel size (8 m²). The wing architecture can vary from 3 panels up to 7 panels per wing, providing up to 15kW End-Of-Life with SHARP silicon cells.

Definitions



For the purpose of using a common vocabulary when speaking about discharges and arcs, here are some definitions:
Primary discharge: The primary discharge is a spontaneous electrostatic discharge lasting some few microseconds. It is also called "blow-off".
Secondary arc: The secondary arc is an arc occurring in the gap between two cells (precisely at the coverglass/cell junction). It is a direct consequence of the primary discharge and is intimately linked to it. It may be either almost simultaneous or slightly delayed with regard to the primary discharge.
The non auto-powered arcs have a duration that is limited to that of the primary ESD.
Auto-powered secondary arc: This is a secondary arc which has a duration longer than the blow-off. The available solar array power is feeding the arc by deriving current in the inter-cells gap. The duration may be up to a few milliseconds but the arc finally self-extinguish without damaging the coupon.
Sustained arc: This is an auto-powered secondary arc which do not self-extinguish. Its duration is only limited by protections that may have been implemented on the test equipment, by the operator or because of the appearance of a short-circuit (consequence of the Kapton® pyrolisation) between the strings.

Plasma test versus Electron gun test

Why testing in plasma or ion versus electron gun ?
Many reasons have led ALCATEL SPACE to use a plasma test instead an electron gun test.
The first time we tested a solar array with a classical electron gun test set-up, we were not able to reproduce some in-orbit anomalies … while it was easy to reproduce them with a plasma test set-up.
The second reason is the difficulty to charge properly the coverglasses on ground in order to obtain a discharge : it can take hours before having a discharge in the gap ! Even if you do not let the current heating improperly the cell.
The third reason is that a solar array can face a plasma environment during its transfer to the geostationary orbit or if an electric thruster is used on board.
Nevertheless, ALCATEL SPACE is aware that testing in electron gun is more representative that testing in plasma at the geostationary location. This is why ALCATEL SPACE has provided 2 solar array samples to ONERA/CNES and KIT in order that further investigations can be carried out using electron gun tests [1] [3].

The ONERA has performed many tests with ions instead of plasma : no difference has been detected. This is not a surprise because, during a test in plasma, only the ions are involved in the coverglass neutralisation.

The main difference between a plasma test set-up and an electron gun test set-up is the value of the capacitance "Cbias" and the voltage "Vbias" (see figure of the test set-up). In an electron gun test, the capacitance Cbias represents the satellite capacitance and the voltage Vbias is the satellite absolute potential when the discharge occurs.
If we consider a satellite capacitance of 0,8 nF and an absolute potential between –5000 V and –15000 V when a discharge occurs, the stored quantity of charge is between 4 and 12 µC and the energy is between 10 and 90 mJ.
In a plasma test set-up, the voltage Vbias is a parameter that can be fitted to determine the primary discharge rate. Above a threshold, if you increase Vbias, you increase the primary discharge rate. For example, to obtain a primary discharge every 5 minutes, Vbias can be put up to –800 V.
The capacitance "Cbias" shall be representative of the energy that could be released if the test was performed with an electron gun. As a consequence, to obtain energy between 10 and 90 mJ, you shall use a capacitance between 30 and 300 nF.

Another difference between plasma and electrons has been identified : in average, the arc duration is shorter or equal with plasma than with electrons. Nevertheless, in plasma and in the same conditions, you can obtain many arcs of different durations. As a consequence, you can add a criterion in your test procedure : to obtain a sufficient number of arcs of duration superior to 100 µs, for example.
The arc impedance is the same with plasma or with electron gun.

Testing with plasma or with ion is a convenient method to obtain a sufficient number of primary discharges in the cell gap. One shall fit the biasing voltage and capacitance and be aware that the arc duration can be shorter with plasma than with electrons.

100 V Solarbus Solar Array coupon plasma ESD qualifying test sequence

This ESD test sequence took place in 2003 in ONERA facility with the co-operation of CNES. (A similar test sequence has been performed in 2002 on a similar test coupon).

The purpose of the test was to verify that an ElectroStatic Discharge could not lead to Solar Array permanent short-circuits in nominal configuration.
The main aspects to be covered by the tests were :

1. verify that no discharge is expected when the solar array is surrounded by a cold and dense plasma with an active potential of +100 V versus plasma potential (transfer phase simulation or electric thruster plume).
2. verify the existence of primary electrostatic discharges in Inverted Voltage Gradient mode, with a passive coupon.
3. qualify the coupon for nominal electrical conditions and characterisation of primary arcs (U, I, t).
4. qualify the coupon for severe electrical conditions (including security margins) and characterisation of primary arcs
5. determine experimentally the limits of the test coupon in two steps, one with voltage and one with the string current. The secondary arcs (U, I, t) shall be characterised.

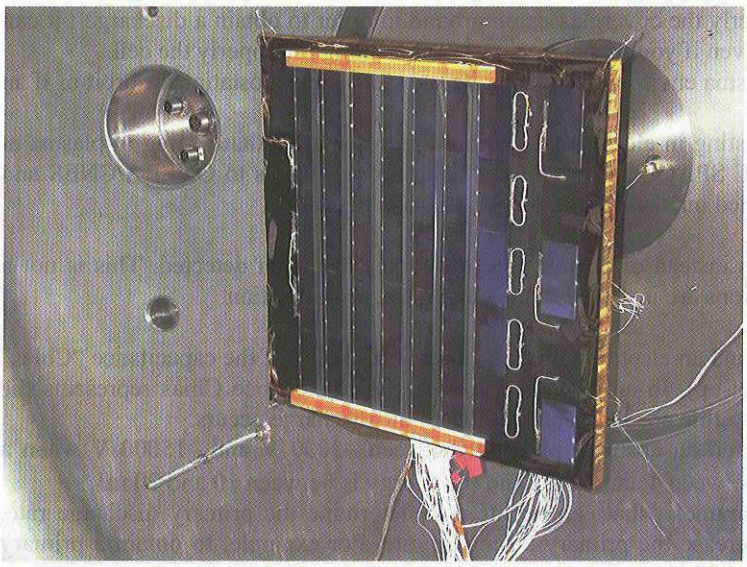
The test coupon was a flight-representative qualification coupon made up with :

- Silicon IBF and Non-IBF SHARP solar cells
- MELCO carbon fibber/honeycomb core sandwich.

The coupon has been manufactured in order to obtain the minimum gap size.
The coupon has been prepared in order to avoid unwanted ESD on the rear face and on the inactive strings :

- strips of transparent polyester films (≈1 cm large) were placed above the cells (≈1 cm above)
- A diaphragm limits the exposure of the coupon to the gap between strings X and Y. It is placed 110 mm away from the coupon.
- The back of the test coupon is "wrapped" in Kapton®

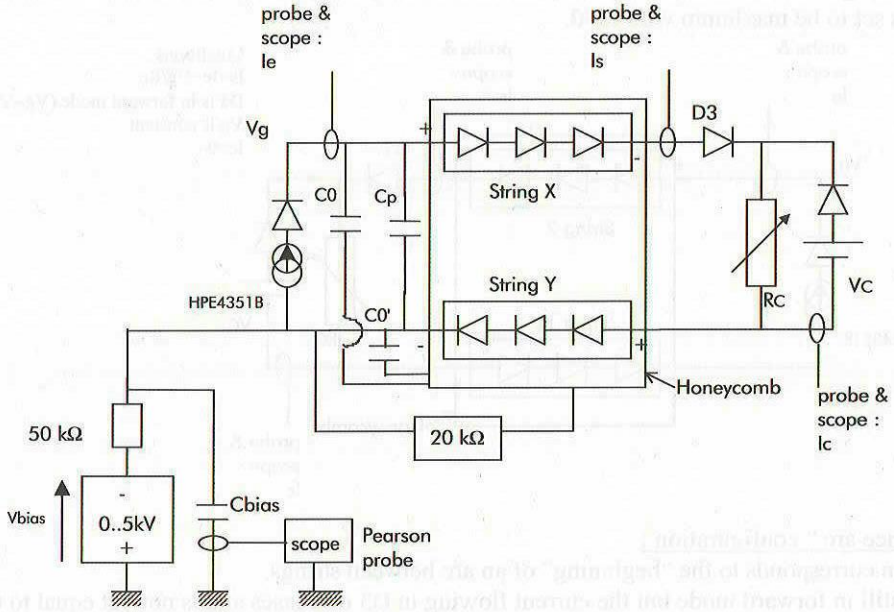
The pictures of the coupon in JONAS chamber are given hereafter.



The test facility was JONAS chamber in ONERA premises :

- dimensions : diameter 1,8 m , length 3 m (volume around 1 m^3)
- Vacuum in the chamber : 10^{-6} mbar range (cryogenic pumping + liquid nitrogen shroud)
- Plasma source, $n_e = 1$ up to 1.10^6 cm^{-3}
- Sample size up to 80 x 80 cm
- High voltage cable feed-throughs (≥ 13 wires, up to 2 kV) to be connected to the SAS and the coupons
- Simultaneous ESD current transient monitoring & recording on 2 and more different lines : Digitalizing Oscilloscope 500 MHz, 2 GS/s and Digital Signal Amplifier able to detect signals as low as 10 mV with a time base of some microseconds
- Visual observation / photography / video of the test sample during test

The CNES Solar Array Simulator (SAS) has been used for the tests with a HPE4351B generator, small capacitance at the exit 50 nF, available power 480 W, (120 V, 4 A).

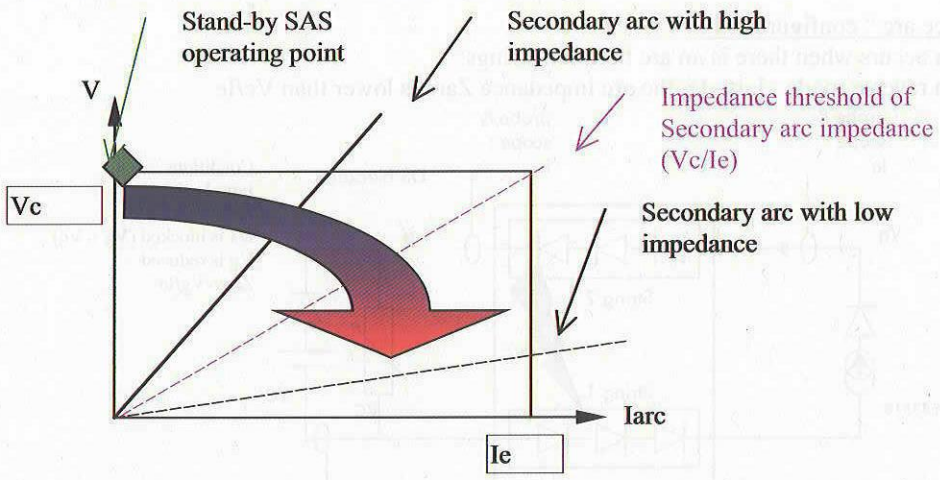


Strings X and Y are the strings under tests, the unused strings are connected to the coupon structure.
The 20 kΩ resistance is the grounding resistance.
The bias capacitance to use is Cbias = 300 nF.
Cp represents the electrodynamic capacity of the solar cell or the string of solar cells.
C0 and C0' represent the capacitance of the solar cells versus the structure.
The capacitances have been put on the rear face of the coupon, as close as possible to the strings, in order to prevent from parasitic inductances that could be induced by long wires.

The discharge detection principle is the result of a fruitful co-operation between CNES, ONERA and ALCATEL SPACE during a previous ESD test campaign. A brief description of the detection principle is given hereafter.
The aim of the SAS is to simulate the electrical string behaviour at coupon level (instead of panel level due to the test facility limitation). The main characteristics to simulate are :

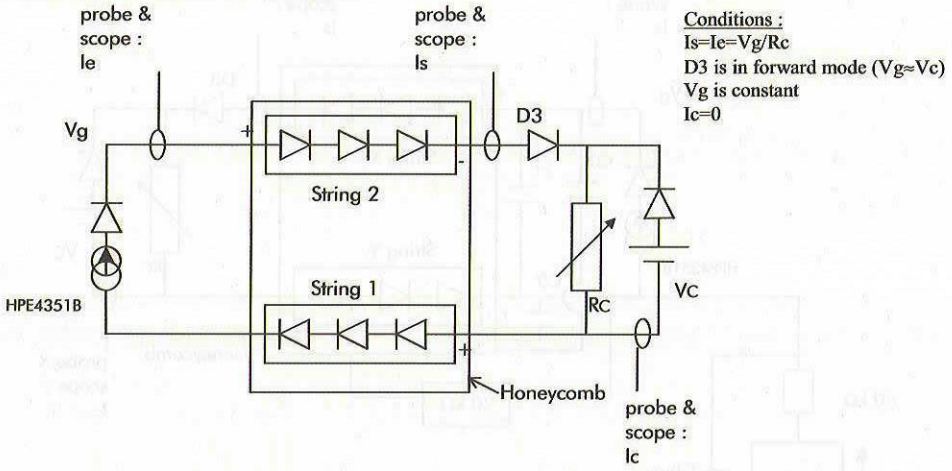
- the differential voltage (between adjacent cells from two different strings)
- the maximum available current (in case of secondary arc)
- the string electrodynamic capacitance

Three operating configurations, as illustrated in the following graphic, are possible for the SAS:



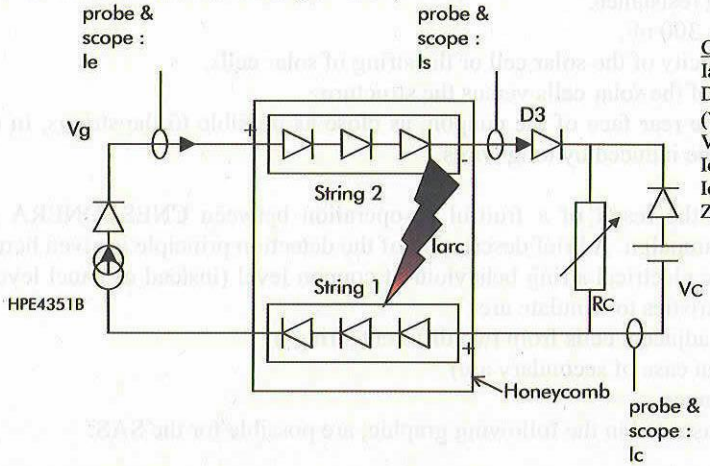
1) "Stand by " configuration

This configuration occurs when there is no arc between strings. The current is regulated by the power supply (current generator). The voltage between cells is driven by the resistor Rc (Vdiff= Rc x I). The diode D3 is in forward mode. The voltage Vc is set to be maximum with Ic=0.



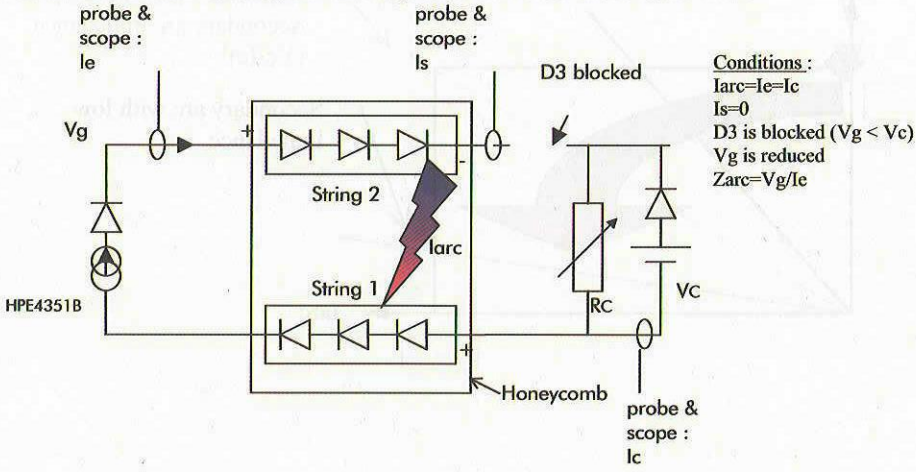
2) "High impedance arc " configuration :

This configuration corresponds to the "beginning" of an arc between strings.
The diode D3 is still in forward mode but the current flowing in D3 decreases and is not yet equal to 0 A.
The diode D3 will be blocked if the arc impedance Zarc is lower than Vc/Ie.
In this case, Ic is the current mirror of Iarc. (Ic = Iarc).



3) "Low impedance arc " configuration :

This configuration occurs when there is an arc between strings.
The diode D3 is in reverse mode : Iarc=Ie, the arc impedance Zarc is lower than Vc/Ie

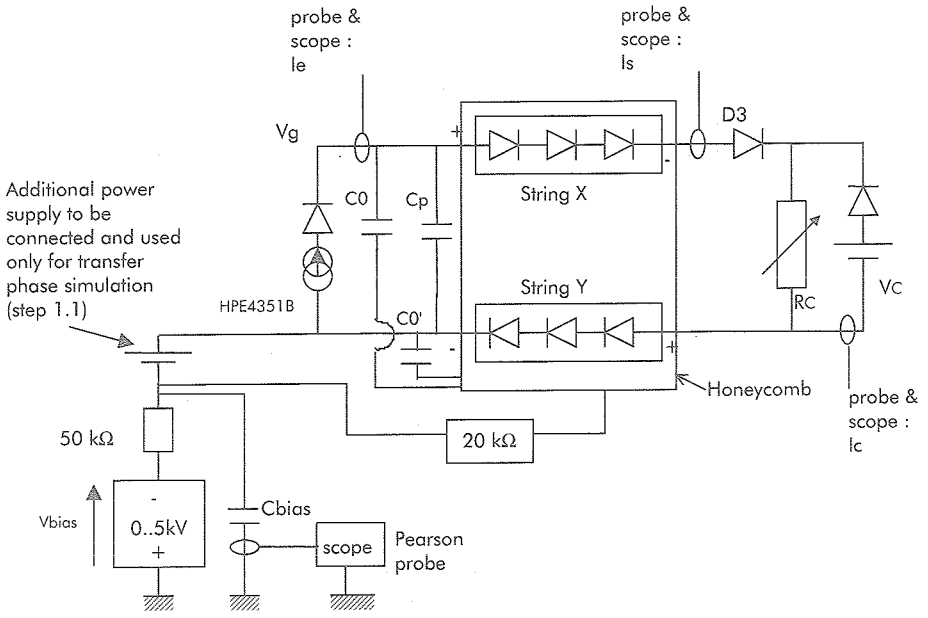


The global test sequence is summarised in the table hereafter:

STEP	TEST Title
	Step 0 : Coupon characterisation before ESD tests
0.1	Gap measurement
0.2	Visual inspection
0.3	Electrical check (① continuity, ② insulation, ③ IBF testing, ④ diodes checking)
0.4	Electrical performance (flasher test)
	Step1 : Transfer phase simulation and V_{bias} determination
1.1	Test on coupon polarised at 100 V (transfer phase simulation)
1.2	Determination of V_{bias} on un-polarised coupon
	Step 2 : Polarised coupon in nominal configuration
2.1	Test under 33 V and 1.25 A between **strings 2 and 3** (non IBF cells)
2.2	Test under 33 V and 1.25 A between **strings 4 and 5** (IBF cells)
	Step 3 : Polarised coupon in worst case configuration
3.1	Test between **strings 2 and 3** successively with – 40 V and 1.25 A – 50 V and 1.25 A – 60 V and 1.25 A
3.2	Test between **strings 4 and 5** successively with – 40 V and 1.25 A – 50 V and 1.25 A – 60 V and 1.25 A
	Step 4 : Coupon inspection
4.1	Visual inspection
4.2	Electrical check (① continuity, ② insulation, ③ IBF testing, ④ diodes checking)
4.3	Electrical performance (flasher test)
	Step 5 : Margins characterisation
5.1	Characterisation versus voltage: Test successively between **strings 2 and 3** with 1.25 A and 60 V, 70 V, 80 V, 90 V, 100 V, 110 V and 120 V
5.2	Characterisation versus current: Test successively between **strings 4 and 5** with 60 V and 1.25 A, 2 A, 3 A, 4 A, and by step of 1 additional A until a sustained arc occurs

The step 0 is a preliminary but mandatory step before the tests. The gap size (=distance between adjacent cells) is carefully measured (accuracy +/- 0.05 mm) because the insulation distance between 2 adjacent cells is an important parameter in the arcing phenomenon [2]. The electrical check and tests are performed in order to be able to identify eventual defects, prior to the test and of course to quantify the defects after the ESD test campaign.

The step 1.1. is devoted to verify that no primary discharge can occur on the solar array when being in a dense and cold plasma. This situation may be encountered in case of an injection at a low altitude (about 200 km) in the ionosphere and in case of the use of an electric thruster at the geostationary orbit.



The different tasks for this step are listed hereafter :
- Outgassing of the coupon in the best possible vacuum (<3.10^{-6} mbar) during 1 or 2 hours.
- Regulate the sample bias to –10 V
- Regulate the "additional power supply" to +80 V
- Apply conditions to the test coupon: +60 V voltage difference between strings 2 and 3, set the available current of the string to 1,25 A (end of string 3 is then +140 V with regard to honeycomb and +130 V with regard to plasma).
- Expose to the cold and dense plasma environment ($n_e \approx 10^6$ cm^{-3}). Due to the polarisation of the coupon, this density may be difficult to achieve, the specification is thus to be as close as possible to the value of $n_e \approx 10^6$ cm^{-3}.
- Verify that no discharge appears during at least 2 hours.
- After exposure, verify that all strings are isolated against each other and against structure.

The purpose of step 1.2. is to determine the value of V_{bias} leading to a discharge rate lower than 5 minutes on the coverglasses.
The different tasks for this step are listed hereafter:
- Removing of the additional power supply from the SAS.
- Outgassing of the coupon in the best possible vacuum (<3.10^{-6} mbar) during 48 hours.
- Exposure to a thin plasma environment ($n_e < 10^5$ cm^{-3}) in a best possible vacuum (<3.10^{-6} mbar).
- Bias the test sample by negative voltages, step by step, from –100 V up to -1000 V if necessary, in order to get a discharge rate lower than 5 minutes on the coverglasses. The determined voltage biasing will be called V_{bias}.
- Record of a few typical discharge signatures I(t)

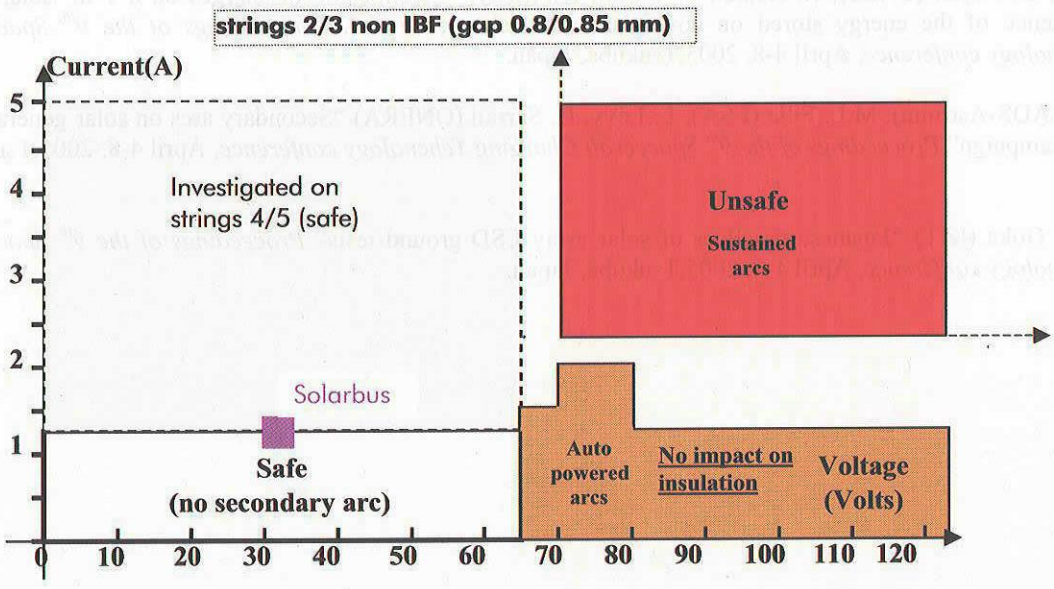
The steps 2.1 and 2.2 correspond to the nominal configuration of Solarbus solar array : 33 V ; 1.25 A. The test sequence duration is 2 hours for each couple of strings.
The steps 3. correspond to a worst-case configuration including a security margin in voltage (in-case of any overshoot in the bus voltage).
The step 4 issues lead to the success criteria of the test.
The steps 5 have not been included in the qualification process of the solar array. They have been performed to identify the design margins. The step 5.2 leads to the destruction of the solar array coupon. Because of heating effects, it is not possible to let 3 or 4 A flowing into the cells. As a consequence, the test set-up has been modified and additional probes were used to detect the arc. More over, the appearance of "secondary auto-power arcs" in step 5.1 around 80 V leads to the modification of the test sequence 5.2. Many extra-work have been performed by the ONERA to be sure to correctly understand all the phenomena.

100 V Solarbus Solar Array coupon plasma ESD test results

During the transfer phase simulation, no primary discharge, and hence no secondary arcs, occurred during the more than 2 hours period of plasma bombardment. This confirms, as foreseen, that no ESD occurs during the transfer phase, when the solar array is surrounded by a cold and dense plasma if polarised at + 130 V max. (100 V S/A) w.r.t. this plasma.

The steps 2 and 3 showed that no primary discharge could evolve into a secondary arc for the tested configurations: 33, 40, 50 and 60 V with 1.25 A. This result confirmed the 3 preceding ESD test campaigns on neighbouring design.
The step 4 showed that the coupon working is exactly the same as before the ESD test campaign : no degradation in insulation and no degradation of the power delivered by the cells have been observed.

During the step 5.1, the new SAS detection principle enabled to discover the existence of "secondary auto-power arcs". These arcs tend to appear around 60/80 V for the smallest gap and were systematic at 90 V. The auto-powered arcs did not lead to any degradation in the insulation. Their frequency and duration increased with the voltage. Their duration was between 30 µs and 145 µs (average 85 µs). At the fixed maximum voltage (120 V; 1,25 A), no sustained secondary arc was detected.
The step 5.2 was modified and performed at 65 V and up to 5 A. More than 500 primary discharges were recorded (more than 200 in the gap) on strings 4 and 5. No secondary arc – even non-auto-powered - was detected. As a consequence, we can say that the arc voltage threshold is the first condition to get a destructive event.
Next, we wanted to know if as soon as non-autopowered secondary arcs are detected, sustained arcs could be obtained by simply increasing the current. The answer to this question seems to be yes : we had only 2 couples of strings and both couples were sacrificed to determine the current threshold at "the auto-powered arc threshold voltage". The "auto-powered arc threshold voltage" depends slightly on the gap distance. The gap sizes were 0,8 – 0,85 mm and 0,9 – 0,95 mm. The smallest gap failed at (80 V; 2,25 A) and the largest at (90 V; 2 A). More over, we noticed that when you increase the current, you increase the average auto-powered arc duration (from 30 µs up to 3 ms). The auto-power secondary arc duration seems to be a good index to feel if you are close or far from the failure.
This result confirmed previous results obtained with neighbouring coupons: 80 V was a threshold in voltage even for smallest gaps (0,56 and 0,68 mm) and the voltage threshold slightly increased when the gap size increased (100 V if 1,1 to 1,5 mm gap). Nevertheless, one shall notice that most of secondary arcs did not occur at the minimum existing gap among the spread between the strings. This suggests that the gap size is of influence but is not the driving parameter.



The Solarbus solar array design offers a security margin of 2 versus the arc voltage threshold (33 V versus 65 V).
The security margin versus the current threshold is also comfortable (1,6) but one shall remind that to get a destructive arc, the first condition is to be above the voltage threshold.
The gap size is the third parameter to control if you want to offer the best protection against the arcing phenomenon. It shall be considered as a minimum insulation distance that is required and controlled.
The values given here only apply to Solarbus solar array design. The arc voltage threshold can be lower (or higher) if you use different Silicon cells.

Conclusion

An ESD solar array test shall be performed with a plasma or ion source. A Solar Array Simulator shall reproduce the electrical behaviour of a solar panel. Only a flight-representative test coupon shall be used. More over, the minimum gap size between adjacent cells shall be tested. Electrical check and performance measurement shall be performed before and after the test, including a flasher test. The test campaign shall lead to the identification of margins versus voltage and versus current.
The SOLARBUS solar array offers a security margin of 2 versus voltage and an additional margin of 1,6 versus current.
The ALCATEL SPACE solar array plasma ESD qualification test procedure is conservative and valid for Silicon cells.

Perspective

Recent solar array ESD investigations (the EMAGS2 study [2]) have shown that some GaAs cells could be damaged by auto-powered secondary arcs that last more than 100 µs whereas Silicon cells are not impacted.
The very last ESD test results performed by Mr. Payan and Al. (CNES) [1] and Mr. Cho and Al. (KIT) [3] show the existence of large flash-over currents lasting more than 100 µs during a primary discharge. The flash-over current is proportional to the panel size.
As a consequence, we consider that the reported solar array plasma ESD qualification test procedure is only applicable to GaAs cells on small panels. CNES, ONERA and ALCATEL SPACE are currently working to modify the test set-up in order to take into account the large flash-over currents.

Acknowledgements

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A special thank to SHARP and MELCO that always provide various samples for ESD tests and are very collaborative to ESD investigations.
We thank Pr Mengu Cho to be deeply involved in establishing an international ESD test set-up.

References

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