CIRCUIT ANALYSIS OF EFFECTS OF SOLAR ARRAY ARCING ON SPACECRAFT POWER SYSTEM

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Abstract

When solar array is operated at a high voltage, arcs occur on the array surface. Our task is to examine the effects of conductive current generated by arcing on solar array circuit of spacecraft. First, equivalent circuits of small solar array module are modeled. The equivalent circuits are made for various types of solar cells such as silicon, gallium arsenic (hetero-junction), and triple junction cells, etc. The equivalent circuit is composed of current source, diode, resistance, inductance and capacitance. First, we measured the frequency characteristic and I-V characteristic of a given solar array, and modeled the equivalent circuit to have the same characteristics by electronic circuit simulation software (SPICE). Next, an electric equivalent circuit of the arc inception was made, and was compared with the ground test result. We simulated the transient current and surge voltage resulted from the ground test using the equivalent circuit. The circuit is being adjusted to experimental results at present. We plan to add the effect of arc expansion to the circuit.

1. Introduction

Recently, arcing on solar array surface was become a serious problem as the scale and duration of space missions get larger and longer [1]. The surge current by the arc may destroy the spacecraft electronic components due to the excessive surge voltage higher than rated. Considering time and cost of experiment for the parts selection, we need to evaluate the influence of the arc. The purpose of the research is to analyze the effect of the solar array arcing on the electric circuit of the spacecraft by using circuit simulation software SPICE. SPICE is a tool which enables a user to design the electric circuit graphically, and to simulate the transition response easily. In this research, we studied an equivalent circuit of a spacecraft including the solar array arcing. The following procedures are included in the study.

(1) Experimental measurement of I/O response to frequency of solar array coupon
(2) Simulation of electrically equivalent circuit by SPICE
(3) Investigation of solar array equivalent circuit including the arc inception

2. Frequency response and diode characteristic of solar array

First, we investigated the frequency response and the diode characteristic of the solar array coupon. We used a solar array coupon made of silicon cells with a conventional design for 100V satellite. IBF (Integrated Bypass Function) is contained in the coupon. Because a silicon solar cell is the same as a diode in dark condition, we can regard the IBF as another diode opposite to the cell.

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The method to acquire the frequency response of the solar array is as follows. A function generator (FG) and a detection resistor (50Ω) are connected to the input and output of the solar array coupon, respectively. The experimental circuit is shown in Fig.1. The frequency characteristic of I/O was measured by the input of a sine wave with various frequencies. We measured the phase characteristic and the impedance characteristic. Figure 2 shows a schematic of relationship between the input voltage and the output current. The phase of the output current shifts from that of the input voltage. The impedance is defined by the amplitude ratio of the input voltage to the output current. It is given by Eq.1.

$$Z = \frac{V_{s\max} - V_{s\min}}{I_{s\max} - I_{s\min}} \quad (1)$$

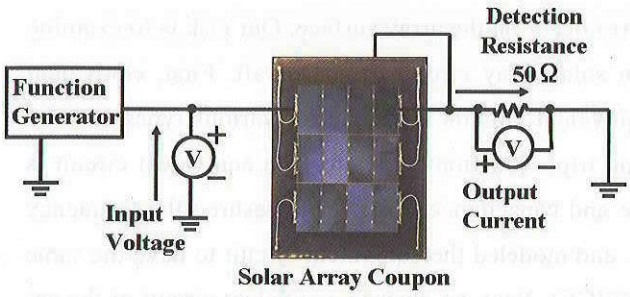

Fig.1 Solar array frequency characteristic acquisition circuit

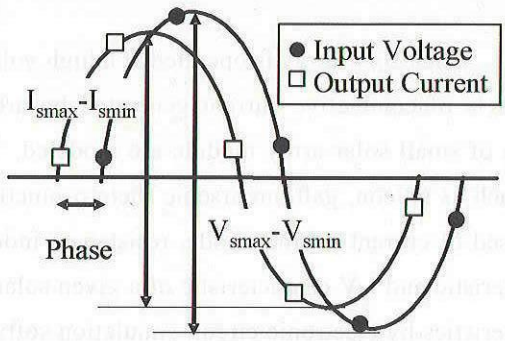

Fig.2 Description of phase and impedance

The diode characteristic of solar array can be acquired by applying variable voltages to solar array in the dark condition. In the dark condition, a solar cell has the same characteristic as a diode. Therefore, the diode characteristic means, in other words, the dark I-V characteristic. When we apply forward bias to the solar array, the diode characteristic of solar array can be acquired. When applying the reverse bias to the solar array, the diode characteristic of IBF, the bypass diode, can be acquired. The diode characteristic acquisition circuit is shown in Fig.3.

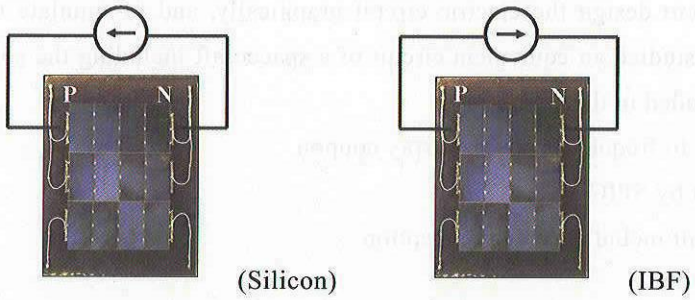

Fig.3 Solar array diode characteristic acquisition circuit

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The acquired characteristics are plotted as the experimental results in Fig.4, 5, and Fig.6.

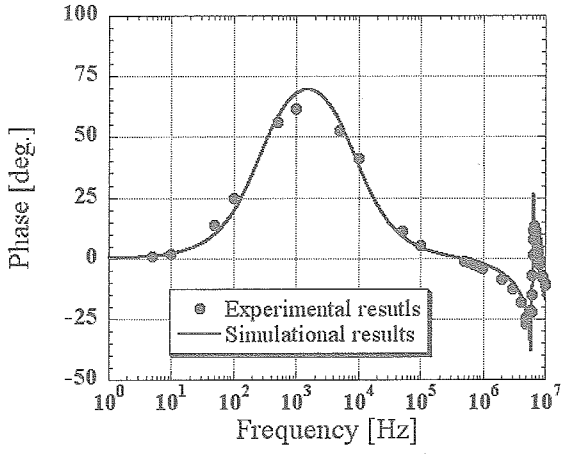

Fig.4 Comparison of simulation result to experimental results (Phase characteristic)

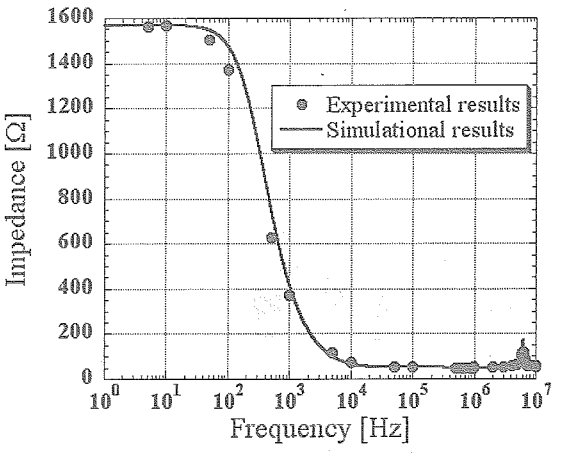

Fig.5 Comparison of simulation result to experimental results (Impedance characteristic)

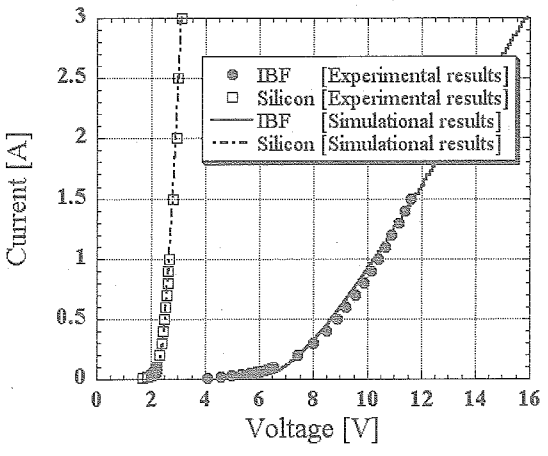

Fig.6 Comparison of simulation result to experimental results (diode characteristic)

3. Simulation results

An equivalent circuit that matched the frequency response and the diode characteristic was designed by SPICE simulation program. The main parameters to be considered in designing the equivalent circuit was PN junction of the solar cell, cover glass, adhesive, insulation sheet (Kapton), IBF, interconnector, etc. Figure 7 shows a cross sectional view of solar array coupon. Figure 8 shows the electrically equivalent circuit corresponding to the structure of the solar array coupon.

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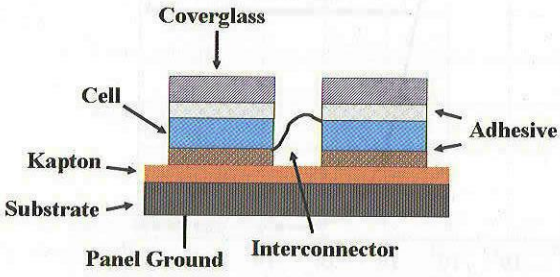

Fig.7 Cross sectional view of solar array coupon

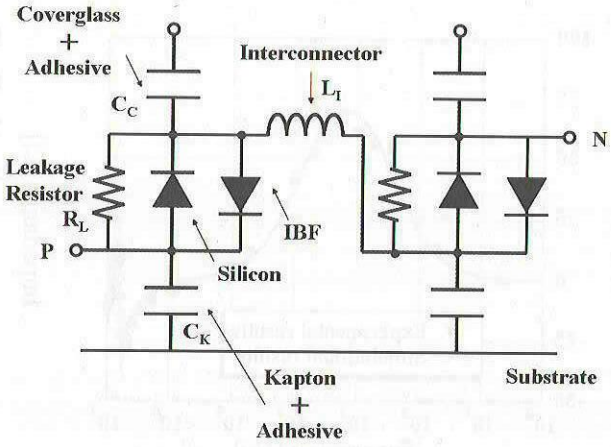

Fig.8 Solar array equivalent circuit

PN junction of silicon and IBF are modeled as diodes connected in parallel. Moreover, leakage resistor R_L of the PN junction is connected to the diodes in parallel. The capacitance of PN junction is included as one of the diode characteristics. The coverglass and the transparent adhesive are connected to the N electrode. Because the coverglass and the adhesive are insulators, they have the capacitance. They are two capacitors connected in series. They are modeled as one capacitance C_C connected to N electrode. P electrode is connected to Kapton and adhesive in series. Because this adhesive and Kapton are insulators, they are connected to P type of the cell as one capacitor C_K. All the capacitors, C_K in the substrate side, were connected to the conductive substrate. The interconnector connecting two adjacent cells has ac inductance component, L_I.

The value of these circuit elements were changed, and simulated by SPICE in order to find the best agreement with the experimental results. We compared the simulated results with the experimental results in the frequency and diode characteristics. The frequency characteristic and the diode characteristic are shown in figure 4, 5, and 6. The characteristic of the solar array measured by experiment is displayed by closed circles in each graph, and the characteristic of the solar array equivalent circuit simulated by SPICE is displayed by the lines. The frequency characteristic shows a very unique characteristic. As shown in these figures, the experimental results and the simulational results agree very well to each other. As for the frequency characteristic, MHz order becomes important because the solar array arcing phenomenon occurs in μsec order. The simulational results show a very good agreement with the experiments in this range of frequency. Diode characteristics of silicon and IBF also show very good agreements with the experiment.

4. Solar array equivalent circuit including arc current

Equivalent circuit including arc current was modeled through comparison with the ground test results. A schematic of the experimental setup is shown in Fig.9. The circuit reproduces inverted potential gradient on solar array and consists of two circuits. One is a circuit which generates an arc. Another is a circuit which simulates the solar array generating power. The circuit, proposed by Payan et al, can simulate electrical response to arcing on solar array adequately [2]. The circuit for arc inception consists of DC power source, V_{bias}, which simulates capacitance of solar array coverglass, and a limiting resistor. The limiting resistor is 100kΩ for power source protection.

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The capacitance, C_{ext}, is called external capacitance and works as a capacitor which supplies energy to the arc plasma. However, the extent to which the plasma can absorb charge from coverglass is not understood well. Therefore, the value of C_{ext} is different for different laboratories ranging from 100pF to 1μF. Capacitor of 6.4nF was used for the ground experiment. The circuit simulating one unit of solar array generating power consists of capacitors C_1, C_2, C_3 and current source I_s. The capacitors C_1, C_2 and C_3 simulate capacitance of 100V solar array. They are 23, 400 and 23nF respectively. The current generator I_s simulates the power generated by the solar array.

The upper two cells of the solar array coupon simulate the positive end of one solar array unit and the lower cells simulate the negative end. The resistor R_L simulates the satellite load. The voltage source CV_{Source} simulates another solar array unit. Blow-off current, line-in current, line-out current, string voltage, and bias voltage are measured as shown in Fig.9. The blow-off current is the current flowing into plasma which absorbs charge of spacecraft surface when an arc occurs. The line-in and line-out current are the currents which flow into the array circuit and the load. The string voltage is voltage between the two strings of the cells. The bias voltage is the charging potential of the spacecraft. Fig.11(a), 12(a) and 13(a) show experimental waveforms when an arc occurred on the upper solar cells.

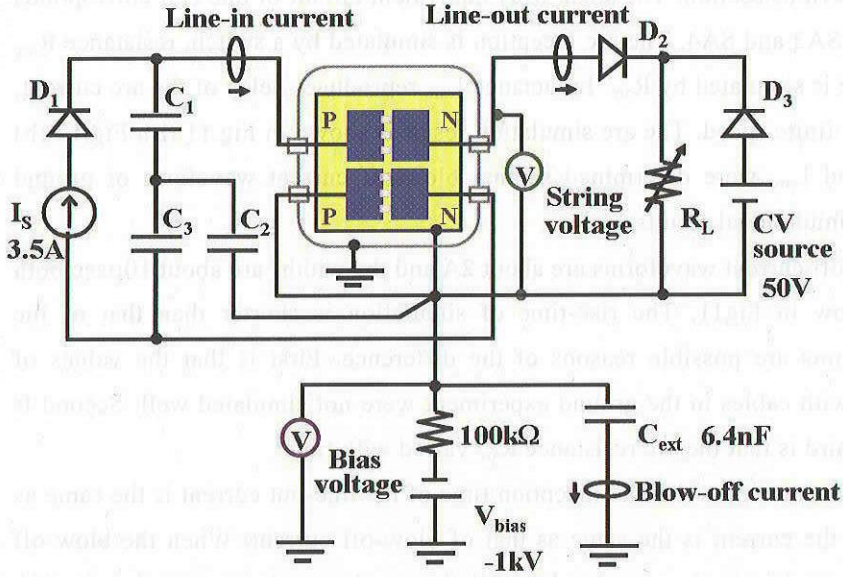

Fig.9 Schematic of ground experiment

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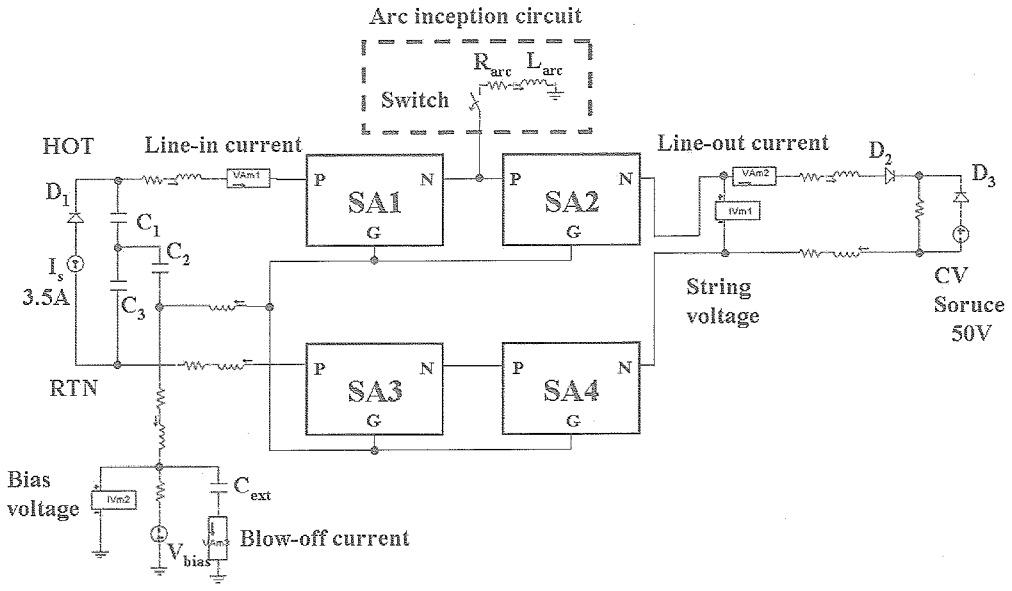

Fig. 10 Solar array equivalent circuit including arc inception circuit that simulates the ground experiment

The circuit for the ground experiment shown above is simulated by SPICE with the solar array equivalent circuit mentioned in the previous section. The solar array equivalent circuit of one cell corresponds to one module, denoted as SA1, SA2, SA3 and SA4. The arc inception is simulated by a switch, resistance R_{arc} and inductance L_{arc}. The arc resistance is simulated by R_{arc}. Inductance L_{arc} reproduces delay of the arc current, because the arc is phenomenon with a finite speed. The arc simulation result is shown in Fig.11 (b), Fig.12 (b) and Fig.13 (b). The value of R_{arc} and L_{arc} were determined so that blow-off current waveform of ground experimental results agreed with the simulational results.

The amplitudes of the blow-off current waveforms are about 2A and the widths are about 10μsec both in experiment and simulation as show in Fig11. The rise-time of simulation is shorter than that of the experiments. The following three points are possible reasons of the difference. First is that the values of resistance and inductance associated with cables in the ground experiment were not simulated well. Second is that the value of L_{arc} was too small. Third is that the arc resistance R_{arc} varied with time.

We simulated the line-out current very well. The inception time of the line-out current is the same as that of blow-off current. Duration of the current is the same as that of blow-off current. When the blow-off current ends, the line-out current approaches to the preset value. All these points were simulated well. The inception time of the line-in current is the same as inception time of blow-off current as well as line-out current. When the blow-off current ends, both of the line-in and line-out currents approach to the preset value. The line-in current decreases when blow-off current begins to flow. The width of line-in current, however, does not agree between the experiment and the simulation. Because the width is influenced by the rise-time of blow-off current, we consider that these widths will agree if blow-off current is simulated well.

In Fig. 12, the widths of surge voltage agree between the experiment and the simulation. The amplitude of surge voltage, however, doesn't agree. The peak of the surge voltage in the experimental is about 170V. The peak in the simulational is about 120V. The peak value of the surge voltage is an important parameter to judge whether a given electronic part can withstand the surge voltage. We should try to match them in future.

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In Fig.13, the bias voltage before arc inception, the experiment and the simulation don't agree because of the voltage drop across the limiting resistor. Except this point, the bias voltage was well simulated after arc inception.

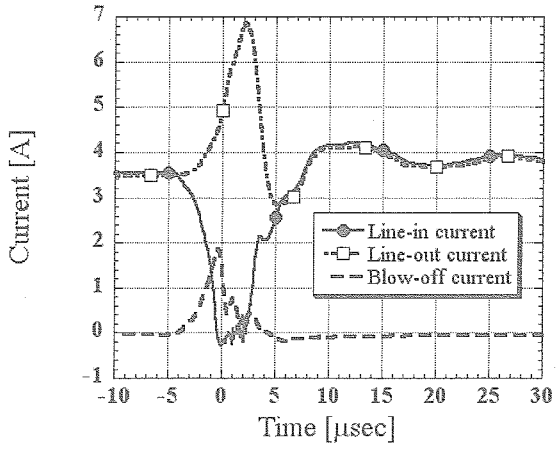

Fig.11(a) Ground experimental results of arc current

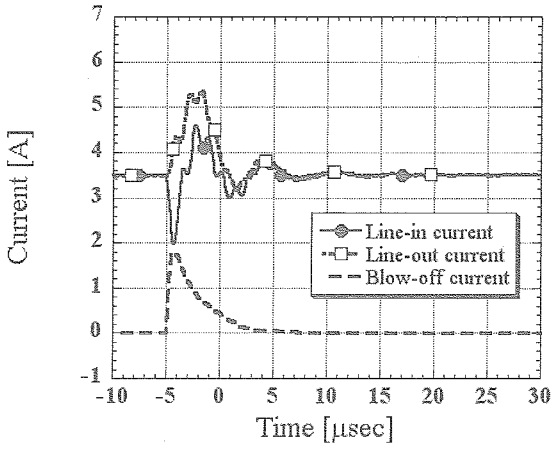

Fig.11(b) Simulational results of arc current

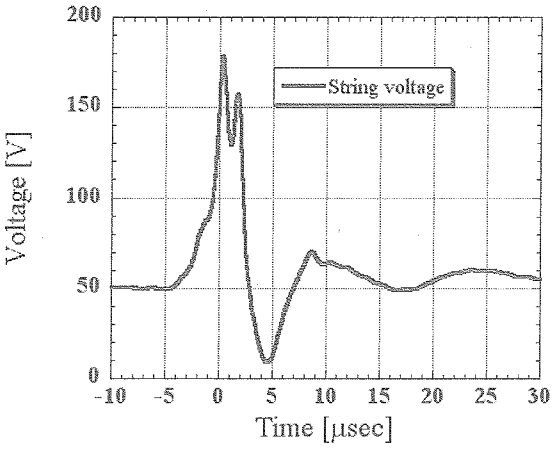

Fig.12(a) Ground experimental results of string voltage

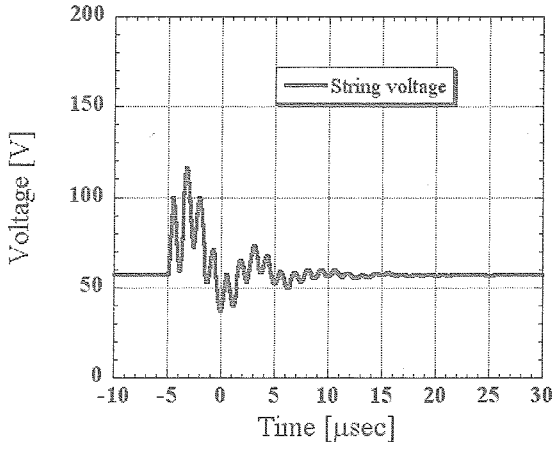

Fig.12(b) Simulational results of string voltage

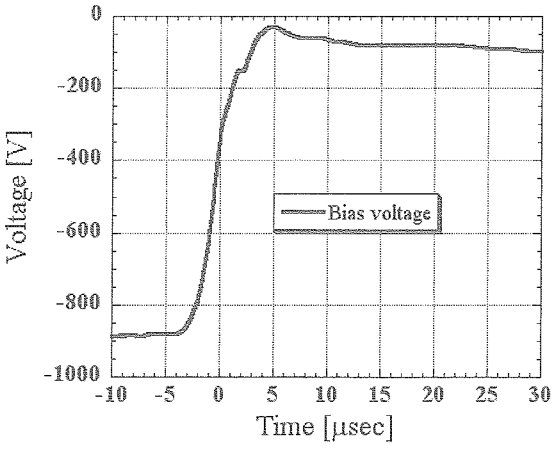

Fig.13(a) Ground experimental results of bias voltage

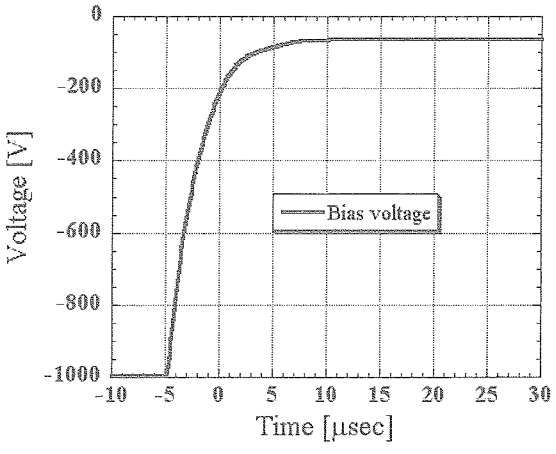

Fig.13(b) Simulational results of bias voltage

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5. Summary

An equivalent circuit of the solar array was developed. The equivalent circuit of the frequency characteristic and diode characteristic was designed by SPICE simulation program. An equivalent circuit including arc was modeled through comparison with results of ground test. The circuit for the ground experiment was simulated by SPICE with the solar array equivalent circuit. The circuit has not been completed yet because the simulational results and experimental results still don't agree completely to each other. Simulating resistance and inductance of cables of the ground experiment, simulating inductance L_{arc} along the arc path, and considering the temporal variation of the arc resistance are necessary in future work.

Acknowledgement

The authors would like to express deep thanks to Mr. Yukishige Nozaki for helpful advice on the SPICE simulation.

References

[1] Cho, M., and Fujii, H., "Review on Charging and Discharging Phenomena in Space Environment: Arcing on High Voltage Solar Array and Future Issues", Aeronautical and Space Sciences Japan, Vol.51, pp.140-145, (2003)

[2] D. Payan, D. Schwander and J.P. Catani, "Risks of low voltage arcs sustained by the photovoltaic power of a satellite solar array during an electrostatic discharge. Solar Array Dynamic Simulator", 7th Spacecraft Charging Technology Conference, April 2001.

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