SOLAR ARRAY PADDLE FOR THE ADVANCED LAND OBSERVING SATELLITE (ALOS): CHARGING MITIGATION AND VERIFICATION

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ABSTRACT

A large solar array paddle with the power generation of 7 kW was developed for the Advanced Land Observing Satellite (ALOS). With the deployed dimension of 22x3m in a polar orbit, this 9-panel rigid paddle has insulator Silver-Teflon thermal sheets and exposed bypath diode boards on its back face, and cover-glass integrated silicon solar cells on its front face. A charging analysis suggested that large negative potentials on the dielectric back-surfaces and at satellite ground may be induced through the ALOS's auroral passage in off-nominal conditions. The ALOS's baseline panel design was tested for the electron beam radiation and the plasma interaction, which simulated charging situations near the poles. Both the back face and the front face were tested, and arc thresholds were identified. Possibility of sustained arc and surge voltage, as well as survivability against estimated accumulation of arcs, were investigated. The back face showed small negative arc thresholds for both the insulator surface potential and the spacecraft ground voltage. Surface flashover was observed over the silver-Teflon coating. Although both the back and front faces demonstrated immunity against sustained arcs, design modifications to mitigate the back face's susceptibility for charging and arcing were experimentally examined and implemented. The conductive adhesive that surrounded the baseline Silver-Teflon sheet and covered the CFRP face-sheets eliminated arcs at the silver-Teflon edges and the face-sheet. The Kapton film shielding the diode board protected the exposed power line from arcs.

1 INTRODUCTION

The Advanced Land Observing Satellite (ALOS) is the high-resolution Earth observation satellite that the Japan Aerospace Exploration Agency (JAXA) developed and will launch this year. This polar orbiting satellite has a large high-power solar array paddle, whose back face is covered with insulator silver-Teflon thermal sheets and exposed bypass diode boards and whose front face is overlaid with cover-glass integrated silicon solar cells, and flies through the aurora zones near the poles.

On October 25, 2003, a JAXA's Earth observation satellite, ADEOS-II, suffered a power failure anomaly and concluded its operation prematurely[8]. Tthe direct cause of the power failure was attributed to aurora charging and a subsequent sustained arc. This accident called Japanese space community's attention to charging of polar orbiting spacecraft and lead to the examination of charging design for the ALOS solar array paddle.

Although severe spacecraft charging in the aurora zones had been observed and reported[10] and various aspects on charging and arcing of solar arrays had been studied for geosynchronous satellites recently[5][6][7], a risk of significant charging and consequential arcs on polar orbiting satellites had not been well recognized by Japanese satellite engineers until the ADEOS-II accident.

The examination of the ALOS paddle revealed a potential risk in its charging design, and lead to analytical and experimental assessments of its charging and arcing characteristics, followed by charging mitigation study. This paper presents an overview of the ALOS paddle design, with a particular emphasis on the characteristics related to charging. A series of the electrostatic discharge tests for the baseline and mitigation designs are summarized with their results.

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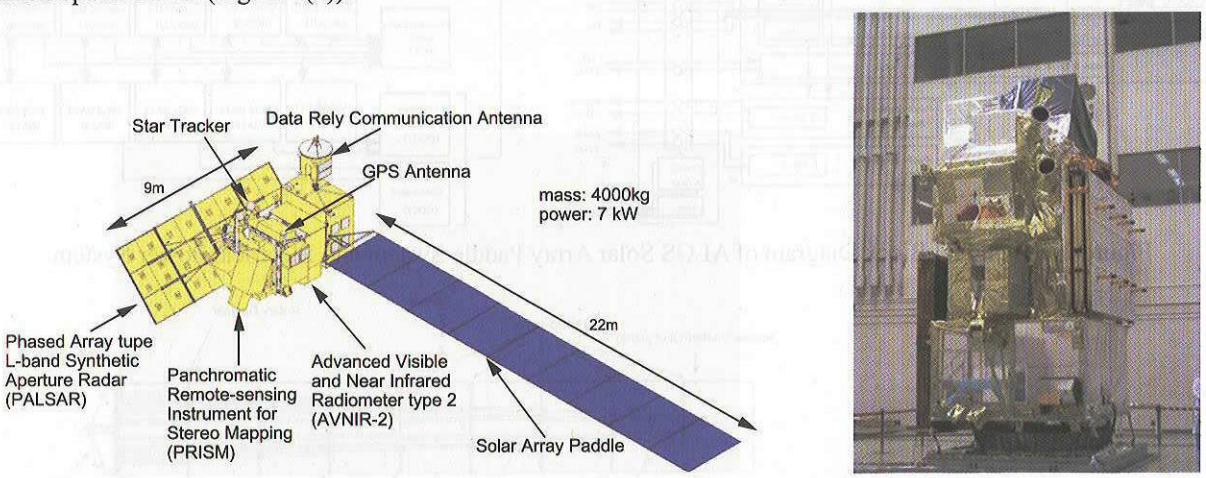
2 ADVANCED LAND OBSERVING SATELLITE

2.1 Mission and Spacecraft

The Advanced Land Observing Satellite (ALOS) is a Japan Aerospace Exploration Agency (JAXA)'s flagship for high-resolution earth observation. Characterized by global data collection with 2.5m resolution, ALOS is given the following mission: cartography, regional environment monitoring, disaster management support, and resource survey. In order to accomplish this mission, ALOS has three mission instruments: Panchromatic Remote Sensing Instrument for Stereo Mapping (PRISM), Advanced Visible and Near-Infrared Radiometer-2 (AVNIR-2), and Phased Array Type L-band Synthetic Aperture Radar (PALSAR). Figure 1(a) shows ALOS's orbital configuration. PRISM is the ALOS's main sensor that consists of three radiometers with 2.5m resolution. AVNIR-2 provides multispectral observation with 10m resolution and pointing capability. PALSAR is a synthetic aperture radar with 10 m resolution and variable off-nadir capability.

With the mass of 4000 kg and the power of 7 kW, ALOS is one of the largest Earth observation satellites that Japan has ever built. This three-axis stabilized satellite will be launched by an H-IIA rocket in September 2005 into a sun-synchronous sub-recurrent orbit with the altitude of 691.65km, the inclination of 98.2deg, and the 10:30 local sun-time of descending node. It will carry out the mission for 5 years. As of today, a series of final electrical qualification tests of the satellite protoflight model, which is the one to be launched, are in progress and near completion at the JAXA's Tsukuba Space Center (Figure 1(b)).



(a) Orbital Configuration (b) ALOS Protoflight Model

Figure 1: Advanced Land Observing Satellite (ALOS)

2.2 Power Requirement

ALOS has subsystems and operations which demand large power generations. The three large observation sensors require the total power of 1.9kW and generate observation data at high rates. These high-rate data are efficiently compressed, coded, stored, and transmitted to ground stations by the Mission Data Handling System (MDHS), which requires the total power of 0.9kW. In addition, power-demanding tight regulation of thermal potentials is necessary for the spacecraft structure and the observation and attitude sensors in order to minimize thermal distortion for precision high-resolution observation.

The global data collection imposed by the ALOS mission requirement inevitably makes continuous observation a premise. That is, continuous and simultaneous observations by PRISM, AVNIR-2, and PALSAR during subsatellite-point daytime and continuous observation by PALSAR during subsatellite-point nighttime are operational requirements for ALOS. These subsystems and operational requirements result in a single-wing solar array paddle generating 7kW at the end of life.

3 ALOS SOLAR ARRAY PADDLE

3.1 Overview

The ALOS Solar Array Paddle System (PDL) has the following characteristics[1]: (1) Single-wing light-weight rigid paddle, (2) Large power generation of 7kW or more @ EOL, (3) Large flexible structure with 9 panels and the deployed dimension of 22.2m x 3.1m, (4) On-orbit life time of 27000 orbital periods or more. The PDL's functional block diagram is given in Figure 2, and its launch and orbital configurations are shown in Figure 3. With 72 array circuits, PDL generates the electrical power of 7kW (@ 55V PDM output voltage) at minimum on orbit over 5 years' mission period. It has the mass of 242kg and consists of 9 solar array panels, a set of hold and release mechanism, a set of deployment synchronization mechanism, a paddle drive mechanism, two sun sensors, and two accelerometers.

Each panel uses a substrate made of CFRP face-sheets and Aluminum honeycomb, and are laid with 36mm x 69mm high-efficiency NRS/BSF silicon solar cells on its face side and silver Teflon thermal sheets on its back side. Eight bypass diode boards and power and signal transmission harnesses are also attached to the back side. The hold and release

mechanism restrains the paddle having the about 30cm thickness with 8 points during the launch, and frees it on orbit by separation nuts. The deployment and synchronization mechanism controls passively deployment angles by synchronization pulleys and cables as well as deployment angular velocities by rotary dampers. It enables the complete deployment within 5min. The electrical power generated by the 9 panels is delivered through the yoke and the Paddle Drive Mechanism (PDM) to the Shunt Unit (SHNT) of the Electrical Power System (EPS). PDM and the Solar Paddle Sun Sensor (SPSS) constitute a feedback loop for tracking the Sun with the Attitude and Orbit Control System (AOCS). Figure 4 shows the PDL protoflight model.

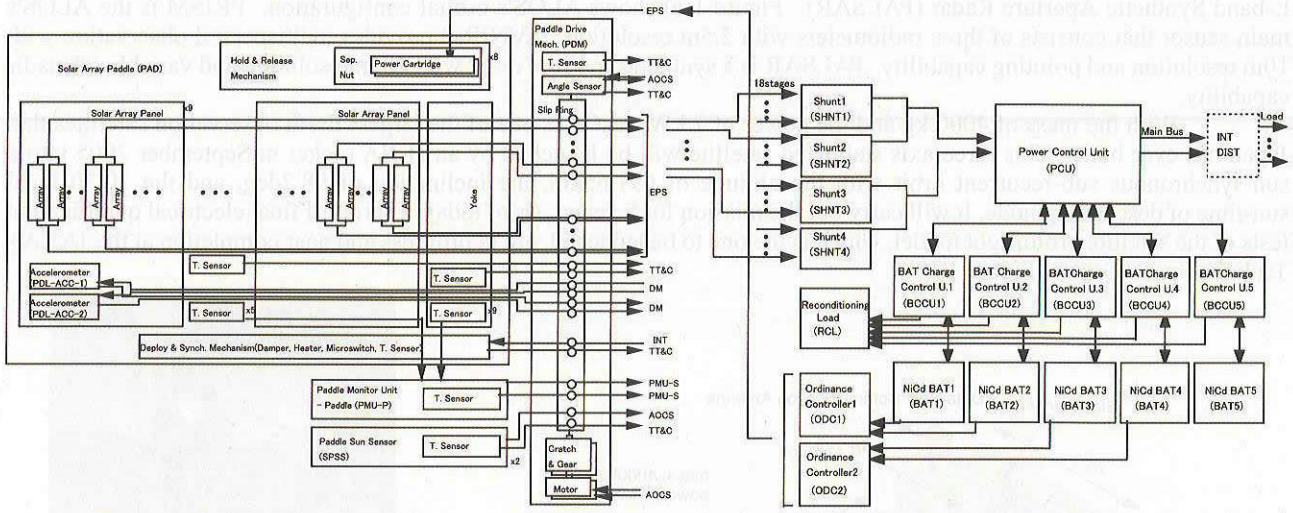
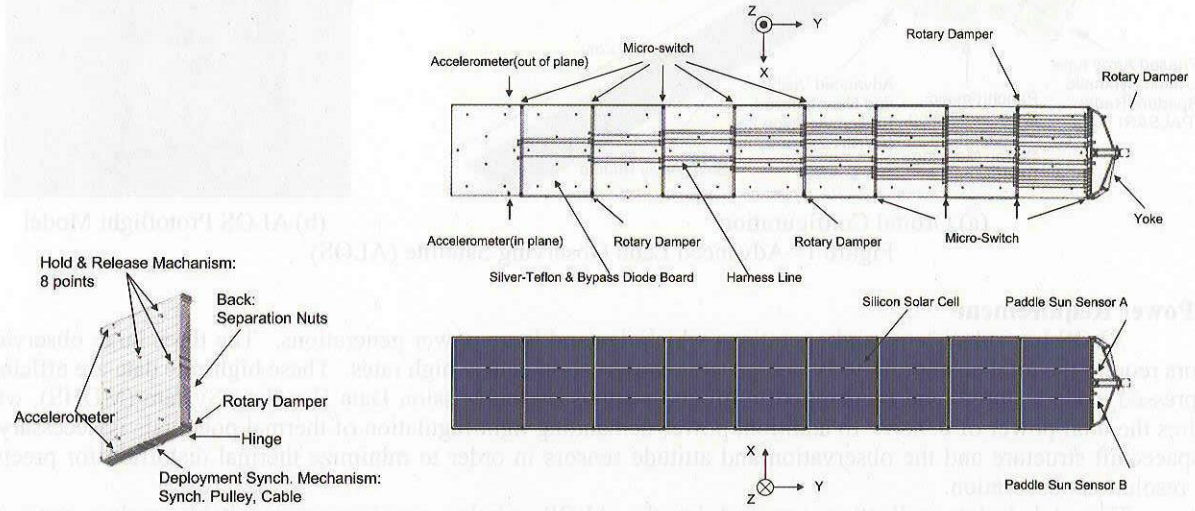
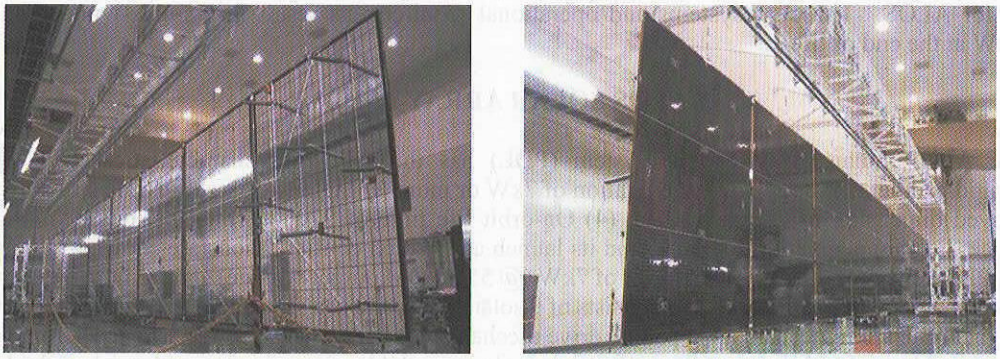


Figure 2: Functional Block Diagram of ALOS Solar Array Paddle System and Electrical Power System



(a) Launch Configuration (b) Orbital Configuration

Figure 3: ALOS Solar Array Paddle



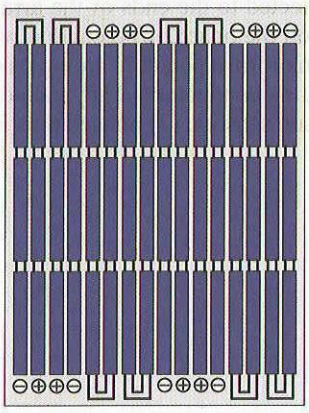
(a) Back side (b) Front Side

Figure 4: ALOS PDL Protoflight Model

3.2 Solar Array Panel and Yoke Design

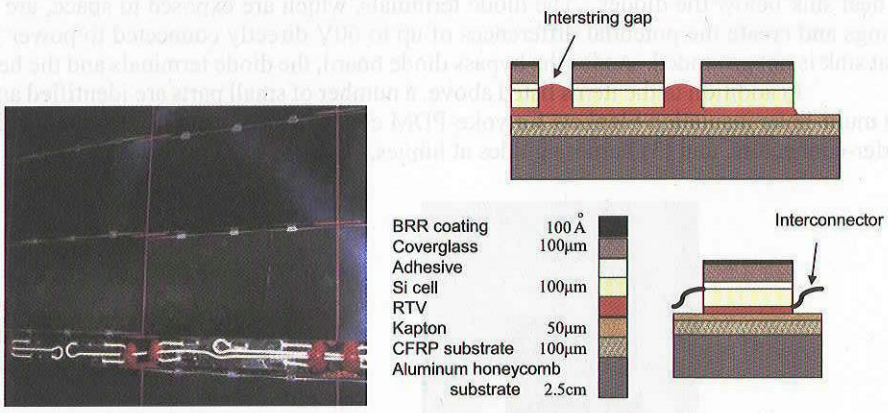
High-efficiency NRS/BSF silicon solar cells with the size of 36mm x 69mm and the thickness of 100 μm are used to achieve the solar array panels efficient to large power generation. Each solar cell is covered with blue red reflection (BRR) coating coverglass to form a coverglass integrated solar cell (CIC) for alleviating temperature rise and improving power output, and is connected to each other by silver inter-connectors. About 23000 cells are attached to the 9 panels and they constitute 72 array circuits of 159 series cells x 144 parallel cells. Each array circuit consists of 6 series strings, and each string has 2 parallel cell circuits to provide the array circuit short current less than 2.8A. Each panel has 8 array circuits, and the locations of their strings are designed to cancel current-magnetic moment (Figure 5). On the array circuit side of the panel, polyimid sheets are attached on the substrate facesheet and below the solar cells to prevent shortcircuit.

In order to protect cells against inverse bias voltage induced by shadows, a bypass diode is connected in parallel to each string, and the resulting bypass diode board that consists of 6 diodes for one array circuit is attached to the panel's back side. Besides the small area occupied by the bypass diode board, most areas of the back side are covered by silver-Teflon thermal coating sheets to improve heat radiation efficiency and subsequently to improve power generation efficiency. The yoke is made of CFRP square tubes, and is coated by white paint to suppress temperature variation and subsequently radiation interference with the satellite main body and PDM.



(a) Cell Layout

Figure 5: Array Circuits Layout



(b) Cross Section

Figure 6: PDL Front Side Design

4 CHARGING ASSESSMENT OF BASELINE DESIGN

4.1 ADEOS-II Accident

On October 25, 2003, a JAXA's Earth observation satellite, ADEOS-II, suffered a power failure anomaly and concluded its operation prematurely[8]. Although the root cause of the anomaly is attributed to an inadequate thermal design for power cables of its solar array paddle, the direct cause of the power failure is due to: (1) the aurora charging of the ungrounded multi-layer insulator that wrapped power cables, and (2) the subsequent sustained arc that burned out the cables at the South Atlantic Anomaly. The accident called Japanese space community's attention to charging of polar orbiting spacecraft.

Prior to the ADEOS-II accident, a risk of significant charging and consequential arcs on polar orbiting satellites flying through the auroral zone and a possibility of substantial temporal/spatial changes in the auroral plasma environment have not been well recognized upon Japanese LEO spacecraft developments. As a result, even common practices in charging design for geostationary satellites have not been strictly implemented for LEO satellites. A lack of charging analysis tools and charging design guidelines for polar orbiting satellites in Japan compounds the problem further. ALOS was not an exception, and the auroral charging had not been addressed for ALOS including its Solar Array Paddle.

4.2 Baseline Design

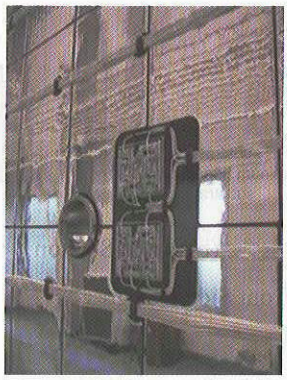
Re-examination of the ALOS design from the charging aspect revealed that ALOS had many small floating conductors in its interior and exterior and that all the surfaces of its thermal control materials were made of insulators without conductive coating. The baseline PDL design, which denotes the ALOS PDL design prior to the ADEOS-II accident, shows charging-related characteristics and potential risks described below.

The face side of the solar array panel is mostly covered with high-efficiency silicon cells constituting 8 array circuits, as the layout in Figure 5 shows. The array's cross section has a layered structure made of 50μm Kapton sheet, 50μm RTV, 100μum silicon cell, 50μm adhesive, 100μm coverglass, and oxidized zirconium coating. Gaps between

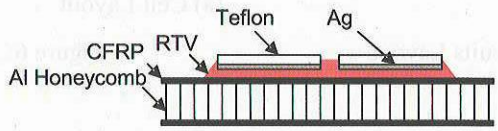
adjacent cells are mostly grouted with nonconductive room temperature vulcanization (RTV) silicon adhesive. Figure 6 shows the inter-cell grouting of the ALOS paddle, where the inter-string gaps are grouted to cover the edges of solar cells, but the interconnectors, the Kapton layer under interconnectors, the bus bars, and the nonadjacent edges of solar cells are not grouted. Each cell produces 1.4A at maximum and resulting array circuit current capability is 2.8A. The maximum voltage of the array circuit and the maximum potential difference between adjacent cells are both 58V (130V or more for circuit's open failure). The generated power of each array circuit is delivered on the back sides of the panels and the yoke by 4 harness lines (2 lines for hot and 2 lines for return). Each array circuit is electrically separated to each other by blocking diodes in the shunt units. As described in the grouting design, the interconnectors, the cell edges at panel borders, and the bus bars are not encapsulated and are exposed to space. Other exposed conductors in the face side include ungrounded dummy cells near hold-down inserts.

The back side of each panel has three major problems. It is mostly covered with 20cm x 10cm silver-Teflon thermal control films and is partially covered with 8 bypass diode boards and wire harness cables transmitting power and signals (Figure 7). The patches of silver-Teflon have the thickness of 51μm and are separated from one another in 2mm spacing. About 3000 films are used for the entire paddle. Since the silver-Teflon film used for ALOS PDL does not have conductive coating for its exposed side and its silver-coated side is attached to the CFRP facesheet by RTV insulator adhesive, the silver-Teflon films pose charging problems of insulator surfaces with significant areas and floating conductors with exposed silver edges. Each bypass diode board has 6 diodes on a glass-polyimide substrate and a pattern of heat sink below the diodes. The diode terminals, which are exposed to space, are connected to the ends of the array strings and create the potential differences of up to 60V directly connected to power line on the board. The conductive heat sink is not grounded. As for the bypass diode board, the diode terminals and the heat sink form a potential arcing risk.

In addition to the items listed above, a number of small parts are identified as floating conductors. They include (1) multi-layer insulation blankets for yoke-PDM connectors, damper heaters, and paddle sun sensors, (2) unused pins in wafer-connectors, and (3) harness guides at hinges.



(a) Bypass Diode Board & silver-Teflon



(b) Cross Section

Figure 7: PDL Back Side Design

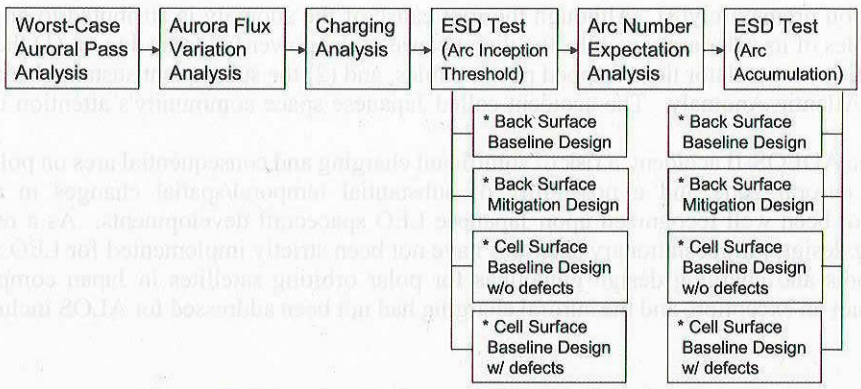


Figure 8: Charging Analyses and Verification Process

4.3 Charging Analysis and Verification Process

The identification of potential risks in the baseline design was followed by a series of analyses and tests to assess worst-case charging potentials of the critical elements and subsequent discharge behaviors. The analyses and tests consist of the calculation of worst-case orbit, the frequency estimation of auroral flux variation, the simulation of charging potentials, the experimental detection of arc inception thresholds, the estimation of expected arc occurrences, and the

laboratory examination of possibility for sustained arc and tolerance to accumulated arcs. The laboratory experiments include the electrostatic discharge tests of front side coupons and back side coupons. The analyses and verification process is summarized in Figure 8.

4.4 Charging Mechanism

Polar orbiting satellites fly through peculiar zones where low-energy high-density ionospheric plasma and high-energy low-density aurora particles coexist[8]. This zone, so called aurora zone, submits a considerable risk to spacecraft charging. For solar array paddles, a combination of the plasma/electron densities in the auroral zone and the paddle's orientation in the polar regions may lead to severe and critical charging events.

As illustrated in Figure 9, near he North and South poles, the paddle's surface is driven to be perpendicular to the flight direction so that the paddle faces directly to the Sun. Plasma wake is formed behind the paddle, where supersonic ionospheric ions can hardly enter but high-energy aurora electrons can penetrate. If the wake side of the paddle has non-conductive surface, the surface can be charged to a highly negative potential[9]. Since exposed conductors in the ram side of the satellite surface collect ions in the plasma flow, the satellite body is well grounded to the ionospheric plasma and has about a negative potential of the solar array output voltage. Therefore, the wake side forms normal potential gradient, in which severe differential charging is possible between insulator surfaces and conductors. This is a typical case for ALOS PDL near the North pole. Near the South pole, the face side with solar cells similarly makes the wake side, but photoelectrons alleviate the negative charging of the non-conductive cell-coverglass.

When the cell side surface faces the ram side near the North pole or the back side surface faces the ram side near the South pole, the surface is exposed to the ionospheric plasma and the surface's potential stays close to the plasma potential. However, if the aurora electron flux becomes significantly high, exposed conductors collect the aurora electrons and the satellite ground can be charged to a large negative potential. In this case, differential charging may occur and inverted potential gradient is formed between non-conductive and conductive surfaces. Table 1 summarizes these cases.

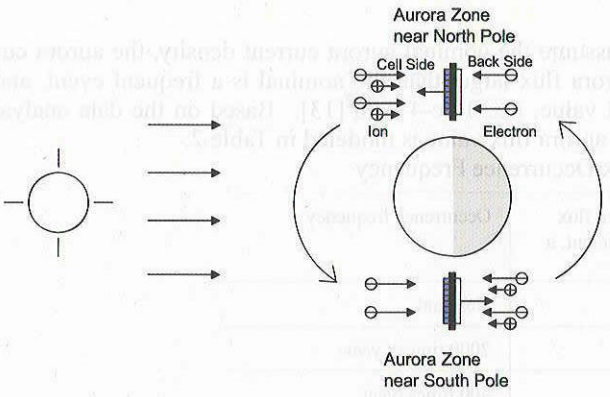


Figure 9: Charging Mechanism

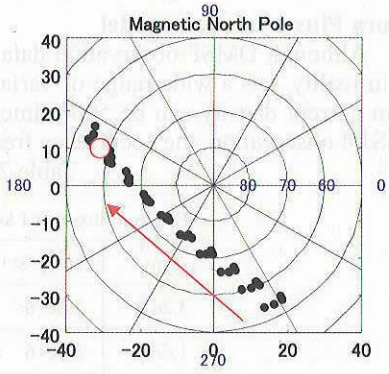


Figure 10: Worst-Case Auroral Passage: Critical Pass on January 30, 2006

Table 1: Critical Charging Cases

	near South pole	near North pole
Back side	**Satellite body** charging Inverted potential gradient	**Silver-Teflon surface** charging Normal potential gradient
Front side	**Coverglass surface** charging Normal potential gradient	**Satellite body** charging Inverted potential gradient

4.5 Worst-Case Auroral Pass Analysis

An orbital analysis was performed to find the auroral passage that may yield the worst-case charging. The conditions for the worst-case charging are assumed to be: (1) fly through the aurora zone continuously as long as possible, (2) stay in the satellite nightside in the aurora zone, (3) enter the satellite dayside right at the exit from the aurora zone, and (4) have the highest geographic latitude when escaping from the aurora zone. Under these conditions, ALOS starts to generate power when the plasma density becomes the lowest and satellite charging reaches the most negative potential. Numerous orbits for one year period were examined and an orbit on January 30, 2006, were found to meet the conditions. Figure 10 shows this orbital pass, and Figure 11 illustrates its geometry. ALOS stays within the aurora zone for about 1200sec, then exits at the geographic latitude of 68deg and the geographic longitude of 86deg (above the Siberia), and immediately enters the satellite dayside. A similar critical pass, in which ALOS stays in the satellite dayside in the aurora zone and enters the satellite nightside right at the exit, was found for the aurora passage in the Southern hemisphere in the same season. Since the year 2006 corresponds to near the minimum in the 11-year period solar activity that gives the

lowest ionospheric plasma density, the January 30 pass may give the worst charging in the mission period. The plasma condition for this worst-case spacecraft position and time is derived from the International Reference Ionosphere, and is used for charging simulations[3]. The assumed plasma parameters include: Plasma density of 2.0e+10m^{-3}, Electron temperature of 0.2eV, Ion temperature of 0.2eV, Averaged ion mass number of 13, Orbital velocity of 7.2km/s, and Nominal aurora current density of 3.2e-8 A/m^2.

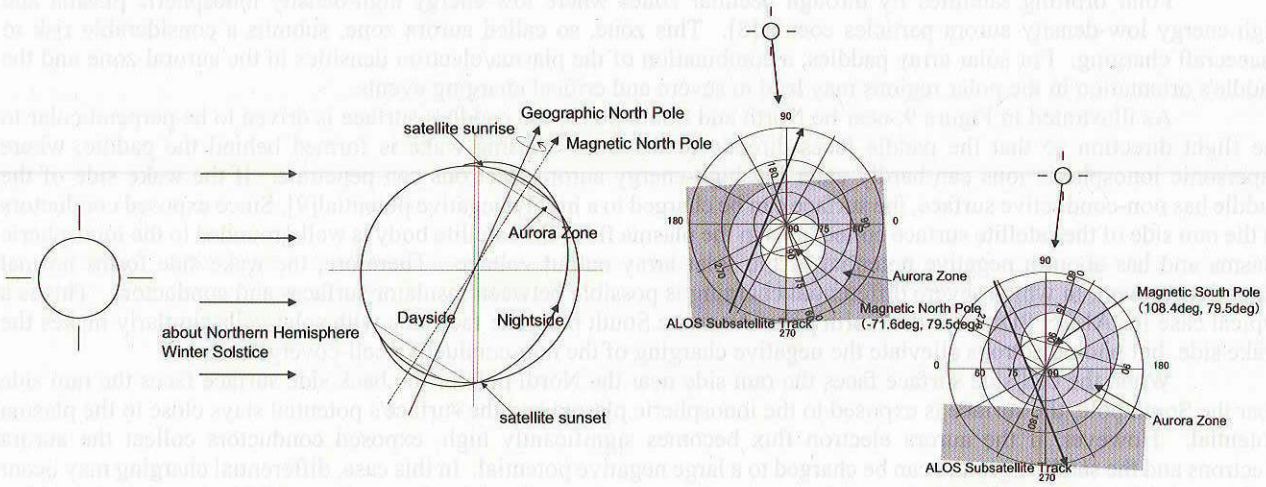


Figure 11: Worst-Case Auroral Passage: Critical Pass Geometry

4.6 Aurora Flux Variation Model

Although DMSP observation data allow us to assume the nominal aurora current density, the aurora current density, in reality, has a wide range of variation. The aurora flux larger than the nominal is a frequent event, and the maximum current density can be 5000 times the nominal value, i.e., 1.6e-4 A/m^2[13]. Based on the data analysis of DMSP SSJ/4 observation, the occurrence frequency of the aurora flux value is modeled in Table 2.

Table 2: Aurora Flux Occurrence Frequency

Electron flux over 1 keV		Aurora flux coefficient, a	Occurrence frequency
A/m^2	cm^{-2}s^{-1}sr^{-1}		
3.2e-8	1.6e+6	1	Nominal
1.6e-7	8.0e+6	5	2000 times / year
1.6e-6	8.0e+7	50	400 times /year
1.6e-5	8.0e+8	500	a few times / year
1.6e-4	8.0e+9	5000	once in every few years

4.7 Charging Analysis

Charging potentials of the satellite body, the coverglass on the face (cell) surface, and the Teflon on the back surface were derived for the aurora passages near the North and South poles by a 0th order analysis. The analysis finds quasi-stationary equilibrium, exploiting macroscopic relations among potential, its temporal change, and incoming/outgoing current flows. Figure 12 shows the resulting charging potentials as a function of aurora current density for the Northern and Southern aurora zones respectively.

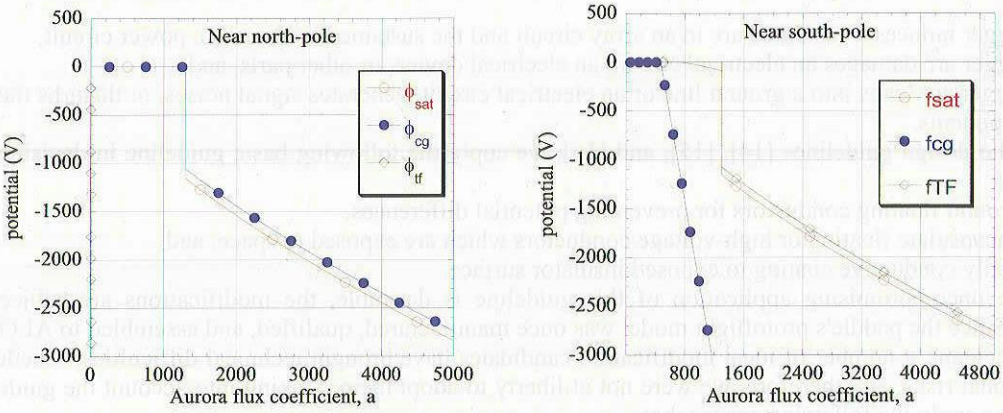
Charging potentials of the paddle's back surface in the aurora zone were computed by means of numerical simulations using a Particle-in-Cell (PIC) scheme and a particle tracking scheme. The two-dimensional simulations provide temporal evolution of the insulator potential in a rectangular computational domain. For details, see the companion paper[2] and only representative results are described here.

Figure 13 represents a potential distribution at 880sec for the nominal aurora current density (3.2e-8 A/m^2). Almost all the back surface shows near zero potential and does not build wake charging. As the nominal aurora current does not build the wake charging, we can expect no arcs on the paddle's back surface in the aurora passage near the North pole.

For the maximum aurora electron current (5000 times of the nominal), significant negative potential is quickly built up on the insulator surface. A potential distribution at 9sec is given in Figure 14, where the back surface potential reaches a surface flashover threshold, -7kV, over the wide back surface area. This suggests that the back side immediately initiates and repeats surface flashover arcs in the worst-case flux environment. A number of simulation runs revealed that

500 times of the nominal aurora current flux is the critical aurora current flux that brings the back surface potential to the surface flashover threshold, -7kV, within 1200sec.

In summary, ALOS PDL does not build significant charging at any medium and low latitude passages and at auroral passages with the nominal space environment. Under the worse space environment, such as geomagnetic storms, the auroral passage may result in severe charging: minus few hundreds volts for the satellite body, and minus few kilo volts for the silver Teflon surface.



(a) Near the North pole (b) Near the South pole

Figure 12: Charging Potentials of Satellite Body, Coveglass, and Teflon

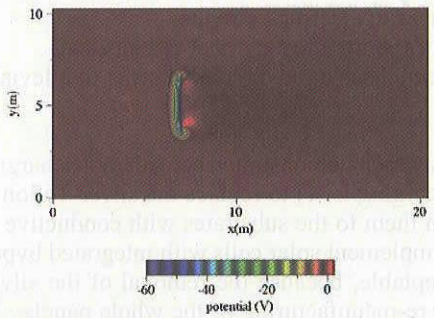
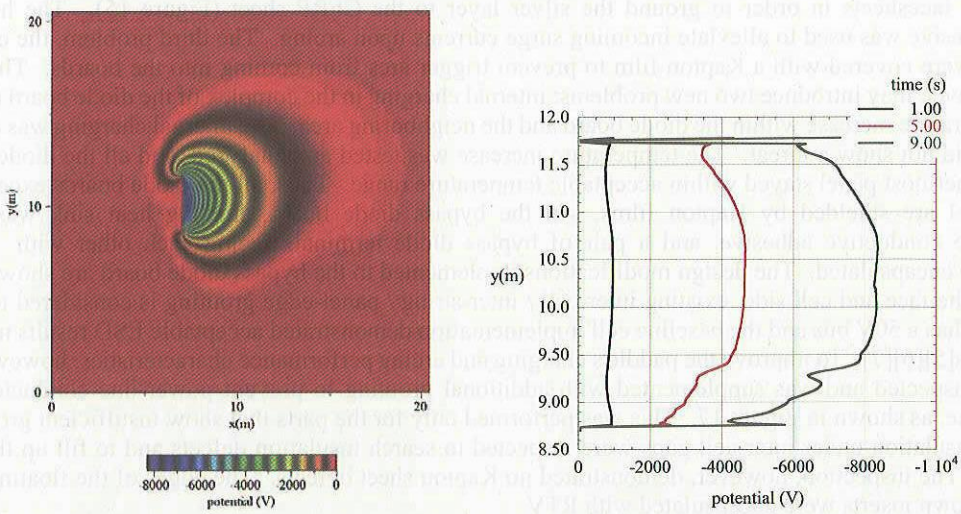


Figure 13: Potential Distribution for Nominal Aurora Current Density (at 880sec)



(a) Spatial Potential Distribution at 9sec (b) Temporal Evolution of Potential Distribution along Back Surface

Figure 14: Potential Distribution for Maximum Aurora Current Density

5 CHARGING MITIGATION

5.1 Mitigation Guideline

The analyses that were shown in the previous section and the laboratory experiments that will be presented in Section 6 demonstrated that the baseline paddle design was susceptible to back surface charging and arcs. Although the baseline design proved its immunity to sustained arc and tolerance to expected arc accumulation, we explored potential modifications to the baseline design in order to mitigate charging and arcing and to improve the paddle's robustness. Our concerns are:

- A trigger induces a sustained arc in an array circuit and the sustained arc breaks a power circuit,
- A trigger arc damages an electrical circuit, an electrical device, or other parts, and
- A trigger arc leaps into a ground line or an electrical circuit, generates signal noises, or disturbs the operation of components.

Referred to the design guidelines [14], [15], and [16], we apply the following basic guideline in devising the paddle's modifications:

- To ground floating conductors for preventing potential differences,
- To encapsulate floating or high-voltage conductors which are exposed to space, and
- To apply conductive coating to exposed insulator surface.

Although the uncompromising application of this guideline is desirable, the modifications are subject to realistic constraints. Since the paddle's protoflight model was once manufactured, qualified, and assembled to ALOS prior to the ADEOS-II accident, a number of ideal modification candidates have brought technical difficulties, schedule problems, and/or additional risks, and therefore, we were not at liberty to adopt them. Taking into account the guidelines and the constraints, we apply the following approaches:

- To enhance a physical barrier between power-line elements with high potential difference, and reduce a possibility of sustained arcs,
- To ground or encapsulate floating conductors in order to reduce an occurrence frequency of trigger arcs and resulting stresses and disturbances to electrical circuits,
- To make a barrier to suppress arc's jump into electrical circuits, and
- To increase an impedance between discharged circuits in order to alleviate peak surge current.

5.2 Design Modifications

For the back side of the panels, which demonstrated considerable charging characteristics in the baseline design, the best and ideal way to mitigate the charging is: 1) to replace the silver-Teflon thermal films with conductively coated silver-Teflon thermal films and to attach them to the substrates with conductive adhesives, and 2) to remove the bypass diode boards from the back side and to implement solar cells with integrated bypass function (IBF) to the face side. This ideal approach, however, were not acceptable, because the removal of the silver-Teflon films and solar cells was not feasible and it would inevitably require re-manufacturing of the whole panels. This constraint results in a compromise that we accept 'as is' one of the three major problems, i.e., dielectric surface of silver-Teflon films. For the floating silver layer, i.e., the second problem, high-impedance conductive adhesive was pasted over the silver-Teflon edges and the exposed CFRP facesheets in order to ground the silver layer to the CFRP sheet (Figure 15). The high-impedance conductive adhesive was used to alleviate incoming surge currents upon arcing. The third problem, the exposed bypass diode boards, were covered with a Kapton film to prevent trigger arcs from coming into the boards. This Kapton film shielding, however, may introduce two new problems: internal charging in the complex of the diode board and the Kapton film, and temperature increase within the diode board and the neighboring area. The internal charging was experimentally studies and it did not show a threat. The temperature increase was tested and analyzed, and all the diode boards except those on the innermost panel stayed within acceptable temperature range. Thus, all the diode boards except those on the innermost panel are shielded by Kapton films. In the bypass diode board, floating heat sink was grounded by high-impedance conductive adhesive, and a pair of bypass diode terminals facing each other with 40V potential difference were encapsulated. The design modifications implemented to the bypass diode board are shown in Figure 16.

For the face and cell side, existing inter-cell / inter-string / panel-edge grouting is considered to be sufficient, because ALOS has a 50V bus and the baseline cell implementation demonstrated acceptable ESD results in Section 6 and in other projects[5][6][7]. To improve the paddle's charging and arcing performance characteristics, however, the existing grouting was inspected and was supplemented with additional grouting to prevent power-line conductors from being exposed to space, as shown in Figure 17. This was performed only for the parts that show insufficient grouting or voids. Kapton sheet insulation under inter-cell gaps were inspected to search insulation defects and to fill up the defects with RTV if found. The inspection, however, demonstrated no Kapton sheet defects. The edges of the floating dummy cells near the hold-down inserts were encapsulated with RTV.

As for other parts of the paddle, the floating multi-layer insulation blankets, which were found at the yoke connector bracket, the rotary dampers, the sun sensors, and the yoke oblique beams, were grounded. The floating harness guides at the panel-to-panel edges and panel-to-yoke edges were also electrically connected in series and were grounded to the substrates. The floating unused pins in the waferconnectors for power and signal lines were capped with thermal-contraction insulator tubes.

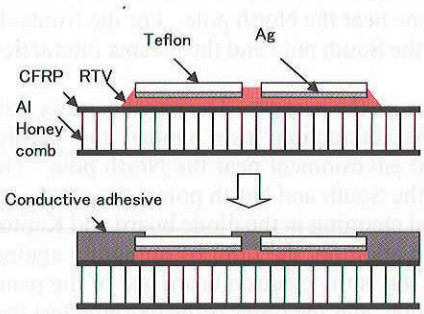


Figure 15: Conductive Adhesive Coating

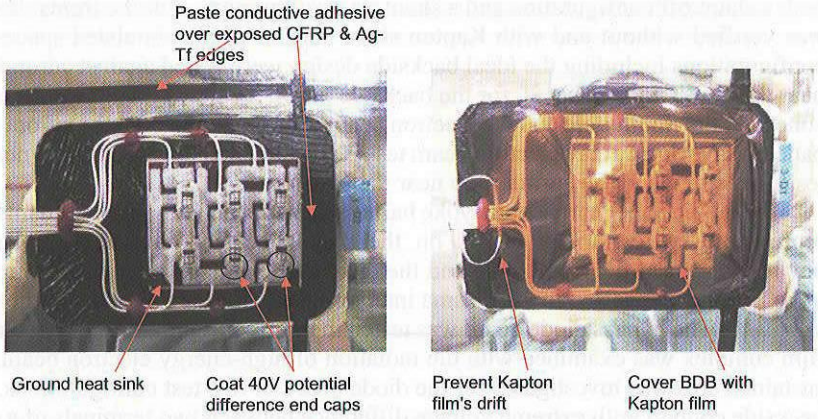


Figure 16: Bypass Diode Board Modifications

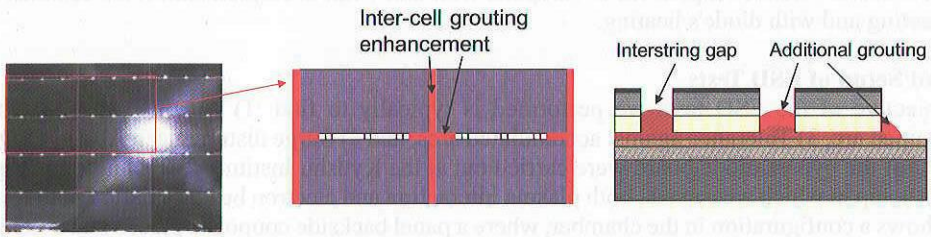


Figure 17: Grouting Enhancement

Table 3: Summary of Tests and Results

Configuration				near South Pole	near North Pole	Results Summary
Panel	**Back side**	Baseline design	Shunt off	**Plasma Interaction Test** Inverted Potential Gradient	**Electron Beam Test** Normal Potential Gradient	- Trigger arc possible in nominal near South pole - No sustained arc - Tolerable against accumulated arcs - Frequent & strong trigger arcs - Surface flashover possible - Disturbance to power line and satellite ground
			Shunt on			
		Mitigation design	Shunt off			- No trigger arc in nominal condition - No sustained arc - Tolerable against accumulated arcs - Less trigger arcs - Surface flashover possible - Mitigated disturbance to satellite ground
			Shunt on			
	Front (cell) side	w/o defects	Shunt off	**Electron Beam Test** Normal Potential Gradient	**Plasma Interaction Test** Inverted Potential Gradient	- No sustained arc - No problem with baseline design
		w/ defects				
Harness	**Panel Back side**	Baseline design	Shunt off	**Plasma Interaction Test** Inverted Potential Gradient	**Electron Beam Test** Normal Potential Gradient	- Trigger arc possible in nominal condition - No secondary & sustained arc
	Yoke Back side	Baseline design	Shunt off	**Plasma Interaction Test** Inverted Potential Gradient		- No arc in nominal condition - Trigger and secondary arcs possible in off-nominal condition - No sustained arc
Bypass Diode Board	**Internal charging**	BDB with Kapton film	Shunt off	**High-Energy Electron Beam Test** Normal Potential Gradient		- Internal charging possible for off-nominal high-energy eletron flux - Long relaxation time - No trigger, secondary, and sustained arc
	Panel Back side, extreme	BDB	Shunt off	-	**Electron Beam Test** Normal Potential Gradient Extreme voltage difference b/w terminals	- No secondary arc with nominal 40V voltage difference - Secondary arc at 110V & sustained arc at 150V
	BDB with laser, extreme	BDB	Shunt off	**Laser-Induced Trigger Arc & Plasma Test** Normal Potential Gradient Extreme voltage difference b/w terminals		- No secondary arc with nominal 40V voltage difference - Secondary arc at 110V & sustained arc at 220V

6 CHARGING VERIFICATION

6.1 Summary of Tests and Results

In order to assess charging and arcing characteristics of the baseline design and improvements of the mitigation design, we performed a series of electrostatic discharge tests and thermal tests. Table 3 summarizes cases and results of the electrostatic discharge tests. We carried out laboratory experiments for the panel backside, the panel frontside, the panel harness, the yoke harness, and the bypass diode board. For the backside of the solar array panel, we examined the baseline design, the mitigation design, and an ideal design. The baseline design and the mitigation design were tested for

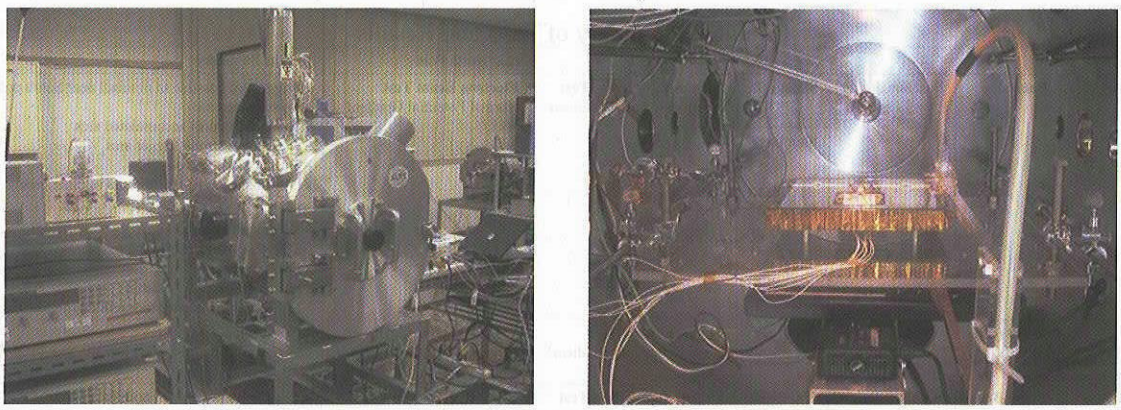
both a shunt off configuration and a shunt on configuration. For the frontside of the solar array panel, the baseline design was verified without and with Kapton sheet defects which simulated space-debris/meteoroid damages. All the panel configurations including the ideal backside design were tested against auroral environment both near the South pole and near the North pole. That is, for the backside panel, we performed the plasma interaction tests that simulated the aurora zone near the South pole and the electron beam tests that simulated the aurora zone near the North pole. For the frontside panel, we carried out the electron beam tests that simulated the aurora zone near the South pole and the plasma interaction tests that simulated the aurora zone near the North pole.

The panel harness and yoke harness were tested with insulator damages on the harness. The panel harness tests representing wire harness cables on the panel backside include the plasma interaction tests against the auroral environment near the South pole and the electron beam tests against the auroral environment near the North pole. The yoke harness was tested in the plasma interaction test for the aurora zones near the South and North poles.

The bypass diode board was tested in three configurations. The internal charging in the diode board and Kapton film complex was examined with the radiation of high-energy electron beam. In addition, the limit of immunity against sustained arcs was investigated for the diode board in two test configurations. One is the electron beam test of the panel backside coupon with extreme voltage difference between two terminals of a diode, and the other is the extreme test that involves laser-induced trigger arcs and resulting dense plasma. For the bypass diode board, thermal tests were performed to find temperature increase due to Kapton film. Coupons with and without Kapton film were examined for two cases: without diode's heating and with diode's heating.

6.2 Objective and Setup of ESD Tests

The objective of the ESD tests we performed is typically to find: 1) Arc inception threshold voltage, 2) Possibility of sustained arc, 3) Tolerance against accumulated arcs, and 4) Surge disturbance. All the ESD tests except the internal charge test of the bypass diode board were carried out at the Kyushu Institute of Technology. Figure 18 shows a typical experiment setup in which we can test both plasma interaction and electron beam radiation in the vacuum chamber. The right figure shows a configuration in the chamber, where a panel backside coupon is placed and a Langmuir probe and an electrostatic voltmeter probe can be identified.



(a) Thermal Vacuum Test Chamber (b) Coupon Setup inChamber

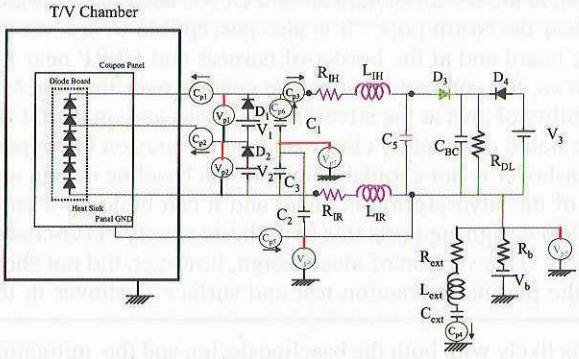
Figure 18: Experiment Setup

6.3 ESD Tests of Panel Backside

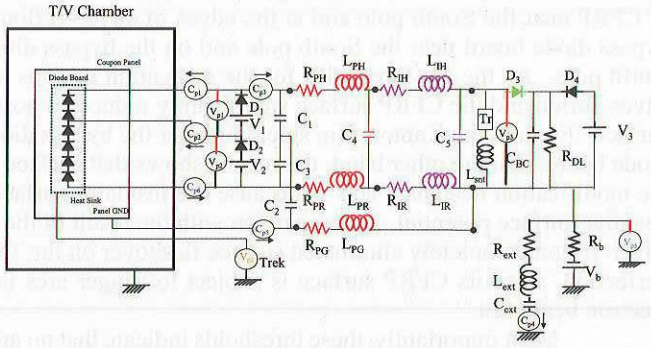
a) Configurations and Coupons

Figure 19 represents electrical block diagrams of the panel backside ESD tests. The shunt-off configuration and the shunt-on configuration are shown both for the plasma interaction tests and the electron beam tests. The shunt-off configuration modeled an innermost solar array circuit, its bypass diode board, a shunt blocking diode, a bus capacitance, a satellite load, and other array circuits, while the shunt-on configuration modeled an outermost array circuit, its bypass diode board, a shunt transistor, a shunt blocking diode, a bus capacitance, a satellite load, and other array circuits. V_b represents the satellite body potential in both configurations, while a capacitance C_{ext} simulates charges stored on other insulator surfaces.

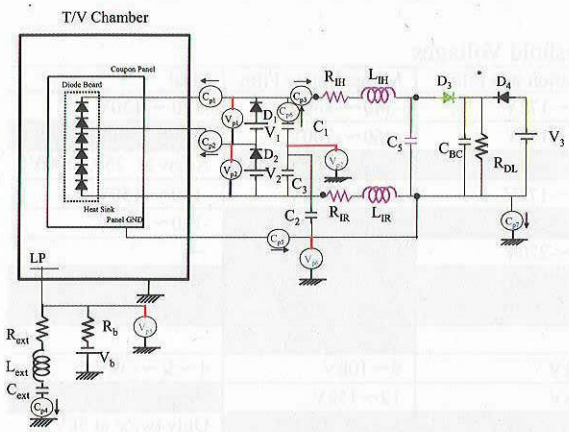
As shown in Figure 20, we prepared four backside coupons, which represent the baseline design, the mitigation design without a Kapton film, the mitigation design, and ideal design. The mitigation design coupon includes all the backside modifications described in Section 5.2. The ideal design includes ITO-coated silver-Teflon grounded by conductive adhesive but does not include a bypass diode board under the assumption of the use of IBF solar cells. It represents the design that we will make when re-manufacturing a panel is possible.



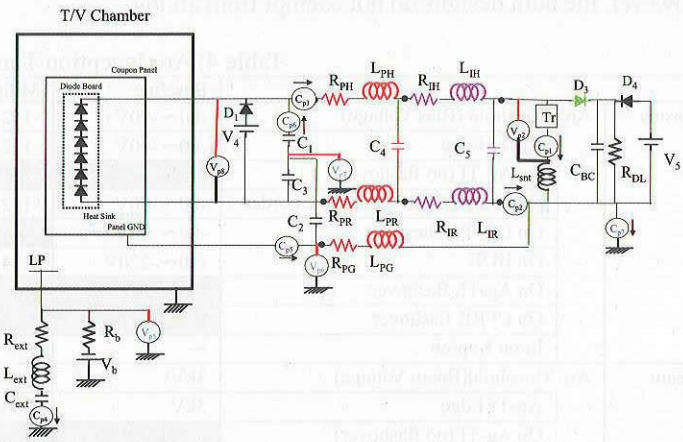
(a) Plasma Interaction Test (Shunt off)



(b) Plasma Interaction Test (Shunt on)



(c) Electron Beam Test (Shunt off)



(d) Electron Beam Test (Shunt on)

Figure 19: Electrical Block Diagrams of Panel Backside ESD Tests

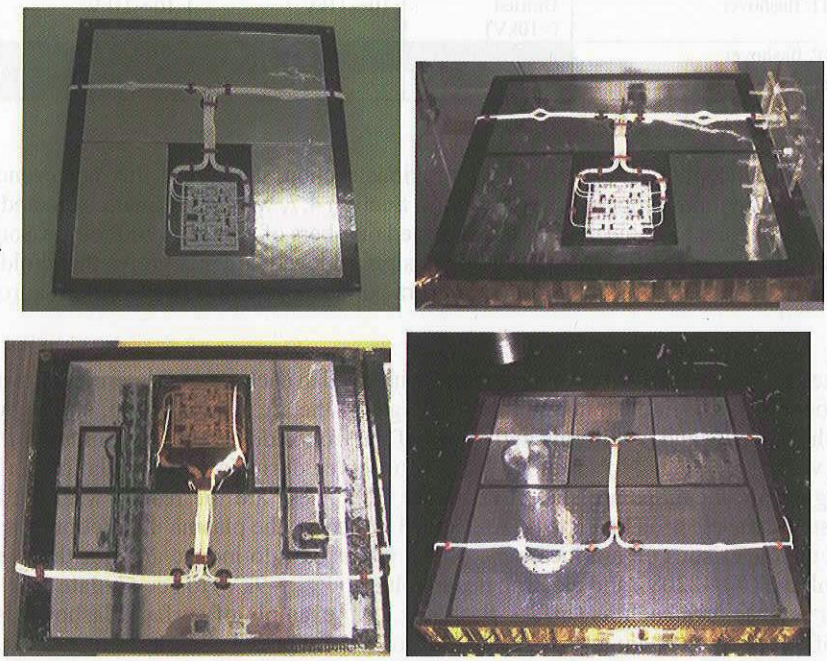


Figure 20: Panel Backside Coupons

b) Arc Inception Thresholds

The arc inception threshold voltages were experimentally identified for the four coupons in the plasma interaction tests and the electron beam tests. Table 4 summarizes the results for the four designs. It was found that each material on the coupons had its own arc inception threshold. The material-dependant thresholds are also shown in Table 4.

The baseline design starts to discharge at the edges of silver-Teflon, at the border of harness and CFRP, and on the surface of CFRP near the South pole and at the edges of silver-Teflon near the North pole. It is also susceptible to arc on the bypass diode board near the South pole and on the bypass diode board and at the border of harness and CFRP near the North pole. As the arc thresholds for the mitigation designs shows, the conductive adhesive coating over the edges of silver-Teflon and the CFRP surface significantly reduced a possibility of arcs at the silver-Teflon edges and on the CFRP surface. Further, the Kapton film shielding over the bypass diode board completely eliminated trigger arcs on the bypass diode board. On the other hand, the results shows that surface flashover is not avoidable in both the baseline design and the modification designs. This is because the insulator surface of the silver-Teflon is intact and it can build up a large negative surface potential. A comparison with the result of the ideal design supports this hypothesis clearly. ITO-coated silver-Teflon completely eliminated surface flashover on the Teflon. This version of ideal design, however, did not show perfection, since its CFRP surface is subject to trigger arcs in the plasma interaction test and surface flashover in the electron beam test.

Most importantly, these thresholds indicate that no arc is likely with both the baseline design and the mitigation design in medium and low latitudes. For the normal aurora environment, the mitigation design shows immunity to trigger arcs, but the baseline design may discharge near the South pole. For the aurora flux due to severe geomagnetic storms, however, the both designs do not exempt from arcing.

Table 4: Arc Inception Threshold Voltages

		Baseline	Mitigation w/o Film	Mitigation w/ Film	Ideal
Plasma	Arc Threshold (Bias Voltage)	-80～-90V+	-152～-172V	-340～-360V	-120～-130V
	Ag-Tf Edge	-80～-90V	-152～-172V	-360～-700V	None (>-900V)
	On Ag-Tf (no flashover)	None (>-220)	None (>-500)	None (>-790V)	A few at -250, -300V
	Harness & CFRP / adhesive border	-80～-90V	-152～-172V	-340～-360V	-130～-150V
	On CRFP/adhesive	-80～-90V	None (>-500)	None (>-790V)	-120～-130V
	On BDB	-90～-220V	-184～-220V	None (>-790V)	—
	On Ag-Tf, flashover	None (>-220)	None (>-500)	None (>-790V)	None (>-900V)
	On CFRP, flashover	None (>-220)	None (>-500)	None (>-790V)	None (>-900V)
	In/on Kapton	—	—	None (>-790V)	—
Beam	Arc Threshold(Beam Voltage)	3kV\	8～9kV	9～10kV	4～5(～6)kV
	Ag-Tf Edge	3kV	8～9kV	12～15kV	None (>20kV)
	On Ag-Tf (no flashover)	None (>10kV)	None (>17kV)	None (>15kV)	Only twice at 5kV
	Harness & CFRP / adhesive border	8～9kV	>10～12kV	9～10kV	4～5kV
	On CRFP/adhesive	Unconfirmed	None (>17kV)	None (>15kV)	5～6kV
	On BDB	8～9kV	11～12kV	None (>15kV)	—
	On Ag-Tf, flashover	Untried (>10kV)	10～11kV	10～11kV	None (>20kV)
	On CFRP, flashover	None (>10kV)	None (>17kV)	None (>15kV)	(5～)6～7kV
	In/on Kapton	—	—	None (>15kV)	—

c) Expected Number of Arcs

Based on the arc inception thresholds in the previous section, the aurora flux occurrence frequency model in Section 4.6, and the rates of temporal potential evolution in Section 4.7, we can estimate expected number of arcs in the 5-year lifetime of ALOS. For the baseline design, the expected numbers of arcs are 1700 for the Southern aurora zone and 23000 for the Northern aurora zone. Since the mitigation design achieved larger negative threshold, it greatly reduces the expected numbers of arcs, that is, 440 for the Southern aurora zone and 1000 for the Northern aurora zone.

d) Arc Accumulation

The expected number of arcs were experimentally induced in each case to determine the possibility of sustained arcs, to identify arc locations, to demonstrate the tolerance against the arc accumulation, and to evaluate surge currents. Table 5 summarizes their results and conditions with those of the front side cases. The number of trigger arcs more than the expected number were generated. No sustained arc was observed during arc accumulations in any cases.

Typical trigger arc locations are shown in Figure 21. These are the results with the baseline design in the plasma interaction test and the electron beam test. As Table 4 indicates, the plasma interaction test and the electron beam test showed different characteristics on arc locations. Since it was easy to induce arcs for the baseline design, we used only moderate bias voltage (V_b=-220V) and electron beam voltage (V_{beam}=9kV) to accumulate arcs. As a result, Figure 21 did not present rather intense arcs such as surface flashover. An example of surface flashover is shown in Figure 22, which is a snapshot of the electron beam test (V_{beam}=15kV) for the mitigation design.

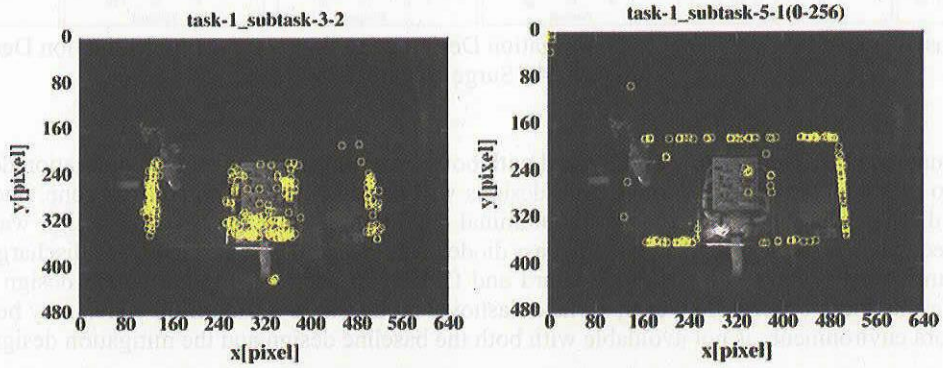
Damages caused by accumulated arcs were inspected and compared with the conditions before the tests. Figure 23 provides examples of the damages on the coupons of the baseline design, the mitigation design without film, and the mitigation design. For each coupon, the right figure shows the damage after the test, while the left figure presents the condition of the same location before the test. Damages at the edge of silver-Teflon, on the silver-Teflon, at the boundary of wire harness and CFRP/conductive adhesive, and at the white coating and diode terminals on the bypass

diode board are typically seen.

Surge currents induced by arcs were also observed. Figure 24 shows typical plots obtained in the electron beam tests for the baseline design (V_{beam}=9kV), the mitigation design without Kapton film (V_{beam}=15kV), and the mitigation design (V_{beam}=15kV). Taking into account that the beam voltage for the baseline design is more moderate than the other cases, we can see that the design modifications alleviate surge currents.

Table 5: Summary of Back Side and Front Side Tests

			South Pole Aurora Zone		North Pole Aurora Zone	
Back Side	Charge Potential	Nominal	Satellite Potential: -60V		Insulator Surface Potential: -280V	
		Worst	Body Potential: Unkown (DMSP: once /1.5 year - 2kV、704 times @<-100V)		Insulator Surface Potential: -9.5kV in 10s (ADEOS: -680V: once/10mnths、AD2 accident: MLI-1.2kV)	
		Gradient	Inverted Potential Gradient		Normal Potential Gradient	
	Test Type		Plasma Interaction Test		Electron Beam Test	
	Design		Baseline	Mitigation	Baseline	Mitigation
	Results	Threshold	Body Potential: -80～-90V	Body Potential: -340～-360V	Surface Potential: -1.5kV	Surface Potential: -7.5～-8.5kV
		Req. #	>1700	>440	>23000	>1000
		Tested #	1500	81 (623 w/ Be coupon)	1500	2719
Cell Side	Charge Potential	Nominal	Insulator Surface Potential: Unknown		Body Potential: -60V	
		Worst	Insulator Surface Potential: Unknown		Body Potential: Unkown (DMSP: once /1.5 year - 2kV、704 times @<-100V)	
		Gradient	Normal Potential Gradient		Inverted Potential Gradient	
	Test Type		Electron Beam Test		Plasma Interaction Test	
	Design		Baseline		Baseline	
	Results	Threshold	Surface Potential: -4.2～-5kV		Body Potential: -100V	
		Req. #	>660		>1000	
		Tested #	1009		1008	



(a) Plasma Interaction Test (b) Electron Beam Test

Figure 21: Trigger Arc Locations: Baseline Design

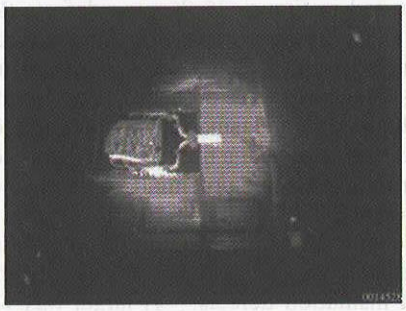
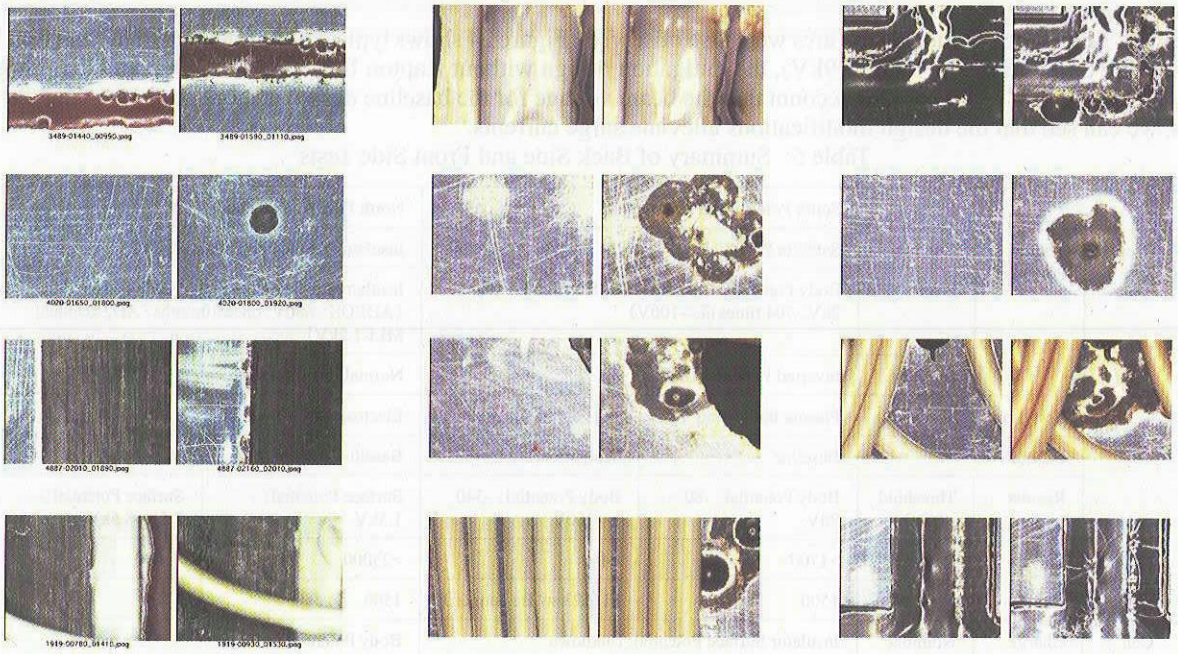


Figure 22: Surface Flashover: Mitigation Design, Electron Beam Test

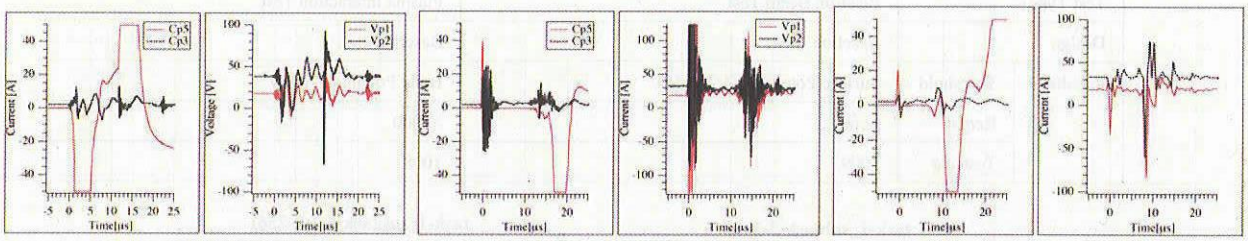


before after
(a) Baseline Design

before after
(b) Mitigation Design w/o Film

before after
(c) Mitigation Design

Figure 23: Damages due to Arcs



(a) Baseline Design

(b) Mitigation Design w/o Film

(c) Mitigation Design

Figure 24: Surge Disturbances

e) Summary

In summary, no sustained arc was observed with both the baseline design and the mitigation designs, and they were tolerable to expected arc accumulation. Both designs will not discharge in non-aurora zone, and the mitigation design will not discharge in the aurora zone in the nominal condition. While the baseline design was susceptible to discharge and frequent arcs were observed on the bypass diode board and CFRP, it was harder to discharge the mitigation design and no arcs were occurred on the diode board and CFRP. In addition, the mitigation design reduced circuit disturbances. Despite these benefits, however, surface flashover on the silver-Teflon film, which may be occurred in the off-nominal aurora environment, is not avoidable with both the baseline design and the mitigation design.

6.4 ESD Tests of Panel Frontside

Figure 25 represents an electrical block diagram of the panel frontside electron beam tests. The panel frontside coupon is shown in Figure 26. As indicated in Figure 25, Kapton defects (knife cut) simulating debris damages are applied to one string in the coupon. The defects were made near interconnectors. With these configurations, the arc inception thresholds were found. An expected number of arcs were estimated and that number of arcs were applied to the coupon. In the accumulation tests, no sustained arcs were observed. For further details, see Reference [4].

Typical trigger arc locations obtained in a plasma interaction test are shown in Figure 27. Trigger arcs often occurred at interconnectors and cell gaps. It appears that a number of trigger arcs were attracted to Kapton defects which exposed the ground potential to neighboring power-line potential. A damage caused by arcs is shown in Figure 28. A sample of surge disturbance is given in Figure 29.

In summary, the panel front side with the ALOS's operational condition (60V) did not yield sustained arc in the electron beam environment with the normal potential gradient and the plasma interaction environment with inverted potential gradient, even if it has Kapton insulation defects. A larger bus voltage (110V), however, demonstrated a sustained arc with Kapton insulation defects.

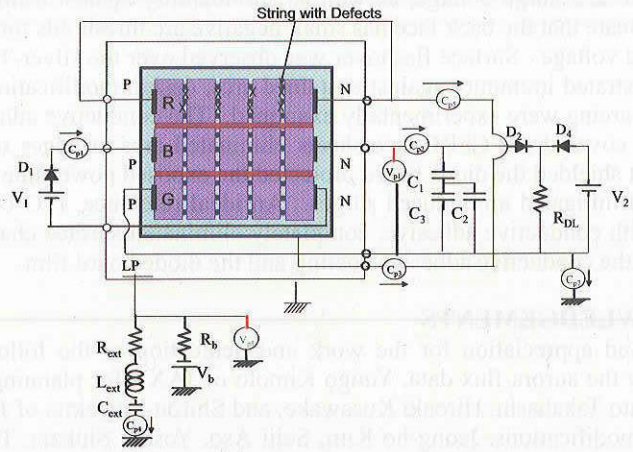


Figure 25: Electrical Block Diagram of Panel Frontside ESD Tests

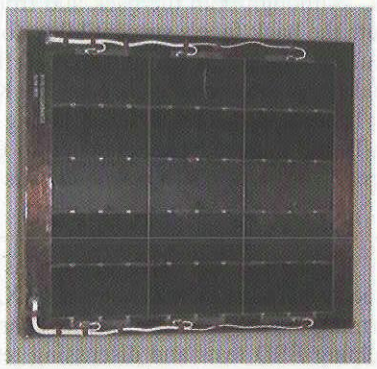


Figure 26: Panel Frontside Coupon

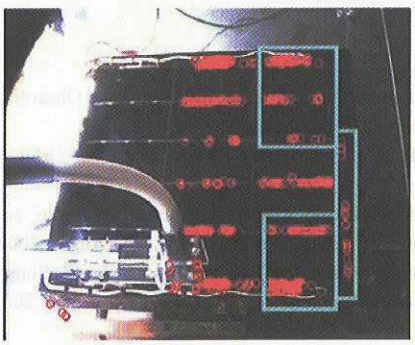
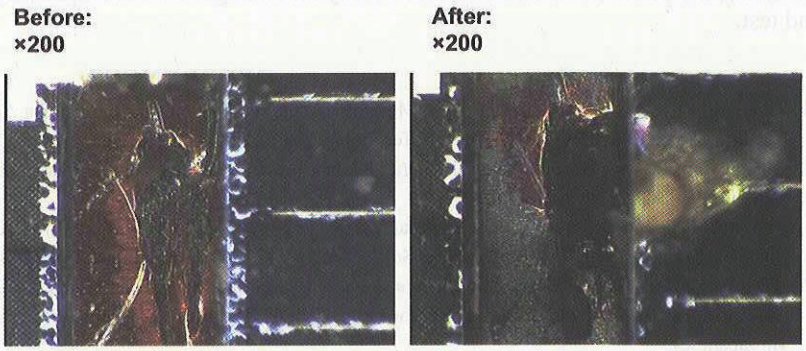


Figure 27: Trigger Arc Locations



before after

Figure 28: Damages due to Arcs

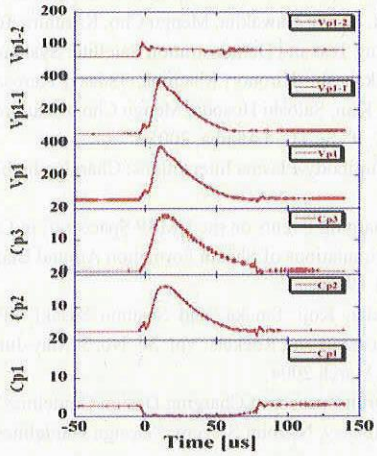


Figure 29: Surge Disturbances

7 CONCLUSIONS

A polar orbiting satellite ALOS has a large single-wing solar array paddle, whose backside surface is overlaid with insulator silver-Teflon thermal sheets and exposed bypass diode boards and whose frontside surface is covered with cover-glass silicon solar cells. An assessment of auroral plasma environment and a charging analysis suggested that large negative potentials on the paddle's dielectric back-surfaces and at satellite ground may be induced through its auroral passage in off-nominal conditions, but no significant charging under the nominal condition. Charging and arcing of the ALOS's baseline panel design was verified in laboratory experiments for the electron beam radiation and the plasma interaction simulating charging situations near the poles. Both the back face and the front face were tested, and arc

thresholds were identified. Possibility of sustained arc and surge voltage, as well as survivability against estimated accumulation of arcs, was investigated. The results indicate that the back face has small negative arc thresholds for both the insulator surface potential and the spacecraft ground voltage. Surface flashover was observed over the silver-Teflon sheets. Although both the back and front faces demonstrated immunity against sustained arcs, design modifications to mitigate the back face's susceptibility for charging and arcing were experimentally examined. The conductive adhesive that surrounded the baseline Silver-Teflon sheets and covered the CFRP face-sheets eliminated arcs at edges of the thermal films and the face-sheets. The Kapton film that shielded the diode board protected the exposed power line from arcs. These approaches reduced arcing possibility and mitigated arc-induced surges. An ideal reference, ITO coated silver-Teflon thermal sheet attached to the substrate with conductive adhesive, completely eliminated surface charging and arcs. The paddle's flight model was modified with the conductive adhesive coating and the diode board film.

ACKNOWLEDGEMENTS

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